

# Technical Datasheet

## AFBR-79EEPZ-HW1-C

### Avago Broadcom® Compatible 40GBase-CSR4 QSFP+ Transceiver

Hot Pluggable, +3.3V, Duplex LC, MPO, DOM, MMF, 850nm, up to 400m,  
Commercial Temperature

#### FEATURES

- 4 CWDM lanes MUX/DEMUX design
- Up to 11.2Gbps per channel bandwidth
- Aggregate bandwidth of > 40Gbps
- Duplex LC connector
- Compliant with 40G Ethernet IEEE802.3ba and 40GBASE-CSR4 Standard
- QSFP MSA compliant
- Up to 400m transmission
- Compliant with QDR/DDR InfiniBand data rates
- Single +3.3V power supply operating
- Built-in digital diagnostic functions
- Commercial Operating Temperature Range: 0 to 70°C
- RoHS Compliant Part

#### APPLICATIONS

- Rack to rack
- Data centres Switches and Routers
- Metro networks
- Switches and Routers
- 40GBase-CSR4 Ethernet Links

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## DESCRIPTION

AFBR-79EEPZ-HW1-C is a transceiver module designed for 400m optical communication applications. The design is compliant to 40GBase-CSR4 of the IEEE P802.3ba standard. The module converts 4 inputs channels (ch) of 10Gb/s electrical data to 4 CWDM optical signals, and multiplexes them into a single channel for 40Gb/s optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 40Gb/s input into 4 CWDM channels signals, and converts them to 4 channel output electrical data.

The central wavelength of 850nm as member of the CWDM wavelength grid defined in ITU-T G694.2. It contains a duplex LC connector for the optical interface and a 38-pin connector for the electrical interface. To minimize the optical dispersion in the long-haul system, single-mode fibre (SMF) must be applied in this module. The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

The module operates from a single +3.3V power supply and LVCMOS/LVTTL global control signals such as Module Present, Reset, Interrupt and Low Power Mode are available with the modules. A 2-wire serial interface is available to send and receive more complex control signals and to obtain digital diagnostic information. Individual channels can be addressed and unused channels can be shut down for maximum design flexibility.

The AFBR-79EEPZ-HW1-C is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

## Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Temperature	T <sub>o</sub>	0		70	°C
Storage Temperature	T <sub>s</sub>	-40		85	°C
Supply Voltage	V <sub>ccT, R</sub>	-0.5		4	V
Relative Humidity	RH	0		85	%

## Recommended Operating Environment:

Parameter	Symbol	Min.	Typical	Max.	Unit
Case operating Temperature	T <sub>o</sub>	0		70	°C
Supply Voltage	V <sub>ccT, R</sub>	+3.13	3.3	+3.47	V
Supply Current	I <sub>cc</sub>			1000	mA
Power Dissipation	PD			3.5	W

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## Electrical Characteristics (T<sub>o</sub> = 0 to 70 °C, VCC = 3.13 to 3.47 Volts)

Parameter	Symbol	Min	Type	Max	Unit	Notes
<b>Data Rate per Channel</b>		-	10.3125	11.2	Gbps	
<b>Power Consumption</b>		-	2.5	3.5	W	
<b>Supply Current</b>	I <sub>cc</sub>		0.75	1.0	A	
<b>Control I/O Voltage-High</b>	V <sub>IH</sub>	2.0		V <sub>cc</sub>	V	
<b>Control I/O Voltage-Low</b>	V <sub>IL</sub>	0		0.7	V	
<b>Inter-Channel Skew</b>	TSK			150	Ps	
<b>RESETL Duration</b>			10		Us	
<b>RESETL De-assert time</b>				100	ms	
<b>Power On Time</b>				100	ms	
<b>Transmitter</b>						
<b>Single Ended Output Voltage Tolerance</b>		0.3		4	V	1
<b>Common mode Voltage Tolerance</b>		15			mV	
<b>Transmit Input Diff Voltage</b>	V <sub>I</sub>	150		1200	mV	
<b>Transmit Input Diff Impedance</b>	Z <sub>IN</sub>	85	100	115		
<b>Data Dependent Input Jitter</b>	DDJ		0.3		UI	
<b>Receiver</b>						
<b>Single Ended Output Voltage Tolerance</b>		0.3		4	V	
<b>Rx Output Diff Voltage</b>	V <sub>o</sub>	370	600	950	mV	
<b>Rx Output Rise and Fall Voltage</b>	Tr/Tf			35	ps	1
<b>Total Jitter</b>	TJ		0.3		UI	

Notes:

1. 20~80%

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## Optical Parameters (T<sub>0</sub> = 0 to 70 °C, V<sub>cc</sub> = 3.0 to 3.6 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
<b>Transmitter</b>						
<b>Wavelength Assignment</b>	L0		830		nm	
	L1		840		nm	
	L2		850		nm	
	L3		860		nm	
<b>Side-mode Suppression Ratio</b>	SMSR	30	-	-	dB	
<b>Total Average Launch Power</b>	PT	-	-	8.3	dBm	
<b>Average Launch Power, each Lane</b>		-7	-	2.3	dBm	
<b>Difference in Launch Power between any two Lanes (OMA)</b>		-	-	6.5	dB	
<b>Optical Modulation Amplitude, each Lane</b>	OMA	-4		+3.5	dBm	
<b>Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane</b>		-4.8	-		dBm	
<b>TDP, each Lane</b>	TDP			2.3	dB	
<b>Extinction Ratio</b>	ER	3.5	-	-	dB	
<b>Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}</b>		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				
<b>Optical Return Loss Tolerance</b>		-	-	20	dB	
<b>Average Launch Power OFF Transmitter, each Lane</b>	Poff			-30	dBm	
<b>Relative Intensity Noise</b>	Rin			-128	dB/HZ	1
<b>Optical Return Loss Tolerance</b>		-	-	12	dB	
<b>Receiver</b>						
<b>Damage Threshold</b>	THd	3.3			dBm	1
<b>Average Power at Receiver Input, each Lane</b>	R	-13.7		2.3	dBm	
<b>Receiver Power (OMA), each Lane</b>				3.5	dB	
<b>Receive Electrical 3 dB upper Cut off Frequency, each Lane</b>				12.3	GHz	
<b>RSSI Accuracy</b>		-2		2	dB	
<b>Receiver Reflectance</b>	Rrx			-26	dB	
<b>Receiver Power (OMA), each Lane</b>		-	-	3.5	dBm	
<b>Stressed Receiver Sensitivity in OMA, each Lane</b>		-	-	-9.9	dBm	
<b>Receiver Sensitivity, each Lane</b>	SR	-	-	-11.5	dBm	
<b>Difference in Receive Power between any two Lanes (OMA)</b>				7.5	dB	
<b>Receive Electrical 3 dB upper Cutoff Frequency, each Lane</b>				12.3	GHz	
<b>LOS De-Assert</b>	LOS <sub>D</sub>			-15	dBm	
<b>LOS Assert</b>	LOS <sub>A</sub>	-30			dBm	
<b>LOS Hysteresis</b>	LOS <sub>H</sub>	0.5			dB	

Notes:

- 12dB Reflection

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## Diagnostic Monitoring Interface

Digital diagnostics monitoring function is available on all QSFP+ CSR4. A 2-wire serial interface provides user to contact with module. The structure of the memory is shown in flowing. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function. The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

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## Timing for Soft Control and Status Functions

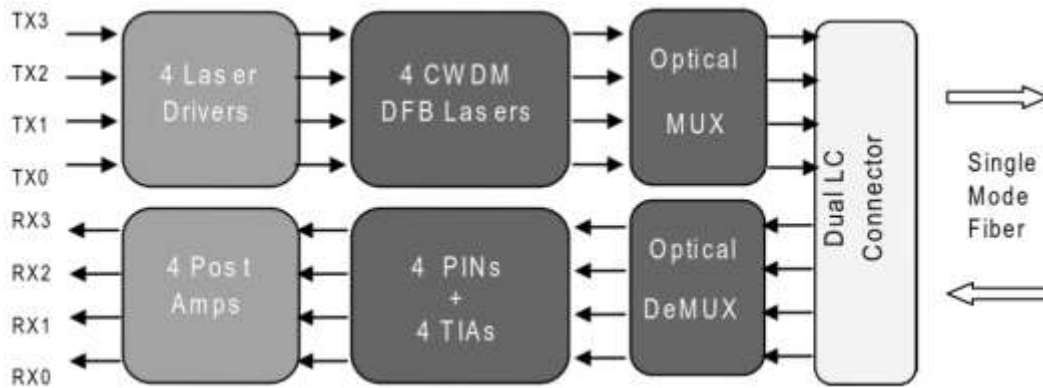
Parameter	Symbol	Max	Unit	Conditions
<b>Initialization Time</b>	t_init	2000	ms	Time from power on <sup>1</sup> , hot plug or rising edge of Reset until the module is fully functional <sup>2</sup>
<b>Reset Init Assert Time</b>	t_reset_init	2	µs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin.
<b>Serial Bus Hardware Ready Time</b>	t_serial	2000	ms	Time from power on <sup>1</sup> until module responds to data transmission over the 2-wire serial bus
<b>Monitor Data Ready Time</b>	t_data	2000	ms	Time from power on <sup>1</sup> to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
<b>Reset Assert Time</b>	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional <sup>2</sup>
<b>LPMMode Assert Time</b>	ton_LPMMode	100	µs	Time from assertion of LPMMode (Vin:LPMMode =Vih) until module power consumption enters lower Power Level
<b>IntL Assert Time</b>	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = Vol
<b>IntL Deassert Time</b>	toff_IntL	500	µs	toff_IntL 500 µs Time from clear on read <sup>3</sup> operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
<b>Rx LOS Assert Time</b>	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted
<b>Flag Assert Time</b>	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted
<b>Mask Assert Time</b>	ton_mask	100	ms	Time from mask bit set <sup>4</sup> until associated IntL assertion is inhibited
<b>Mask De-assert Time</b>	toff_mask	100	ms	Time from mask bit cleared <sup>4</sup> until associated IntL operation resumes
<b>ModSelL Assert Time</b>	ton_ModSelL	100	µs	Time from assertion of ModSelL until module responds to data transmission over the 2-wire serial bus
<b>ModSelL Deassert Time</b>	toff_ModSelL	100	µs	Time from deassertion of ModSelL until the module does not respond to data transmission over the 2-wire serial bus
<b>Power over-ride or Power-set Assert Time</b>	ton_Pdown	100	ms	Time from P_Down bit set <sup>4</sup> until module power consumption enters lower Power Level
<b>Power over-ride or Power-set De-assert Time</b>	toff_Pdown	300	ms	Time from P_Down bit cleared <sup>4</sup> until the module is fully functional <sup>3</sup>

### Notes:

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 de-asserted.
3. Measured from falling clock edge after stop bit of read transaction.
4. Measured from falling clock edge after stop bit of write transaction.

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## Transceiver Block Diagram



## Pin Assignment

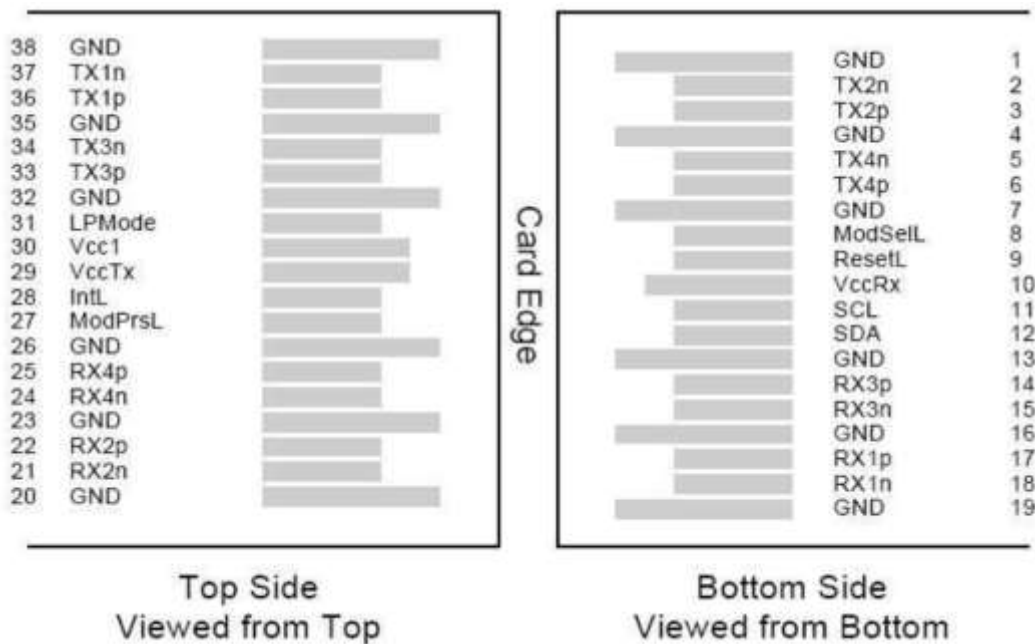


Diagram of Host Board Connector Block Pin Numbers and Name

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## Pin Description

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Output	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Output	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Inverted Data Output	
15	CML-O	Rx3n	Receiver Non-Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Inverted Data Output	
18	CML-O	Rx1n	Receiver Non-Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply Transmitter	2
30		Vcc1	+3.3V Power Supply	2
31	LVTTL-I	LPMODE	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Inverted Data Output	
34	CML-I	Tx3n	Transmitter Non-Inverted Data Output	



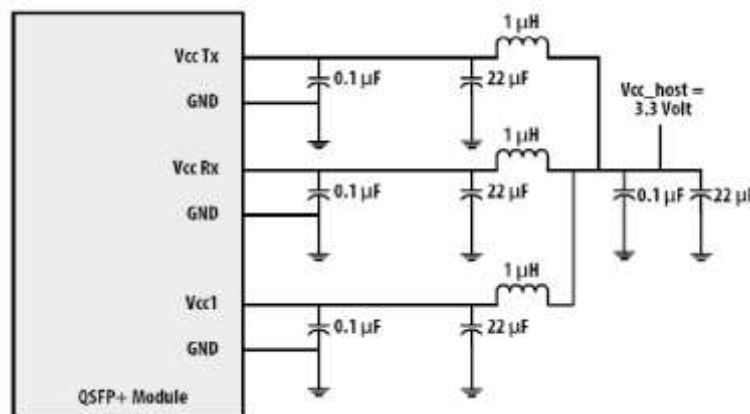
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35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Inverted Data Output	
37	CML-I	Tx1n	Transmitter Non-Inverted Data Output	
38		GND	Ground	1

Notes:

1. GND is the symbol for single and supply(power) common for QSFP modules, All are common within the QSFP module and all module voltages are referenced to this potential otherwise noted. Connect these directly to the host board signal common ground plane. Laser output disabled on TDIS >2.0V or open, enabled on TDIS <0.8V.
2. VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. VccRx, Vcc1 and VccTx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for maximum current of 500mA.

Recommended Circuit



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## Mechanical Dimensions (units: mm)

