

# Technical Datasheet

## QSFP-100G-ZR4-MSA-AT

### Universally Coded MSA Compliant 100GBase-ZR4 QSFP28 Transceiver

Hot Pluggable, +3.3V, LC Duplex, 1295nm to 1309nm, 80km, Commercial  
Temperature

#### FEATURES

- 4 lanes MUX/DEMUX design
- LAN WDM EML laser+ PIN receiver
- Built-in 4-channel Clock and Data Recovery (CDR)
- Integrated LAN WDM TOSA / ROSA for up to 80 km reach over SMF G.652
- Supports 100GBASE-ZR4 for line rate of 103.125Gbps and OTU4 for line rate of 112.2Gbps
- Aggregate bandwidth of > 100Gbps
- Duplex LC connector
- Compliant with IEEE 802.3-2012 Clause 88 standard IEEE 802.3bm CAUI-4 chip to module electrical standard ITU-T G.959.1-2012-02 standard
- Single +3.3V power supply operating
- Built-in digital diagnostic functions
- Temperature range 0°C to 70°C
- RoHS Compliant Part

#### APPLICATIONS

- Local Area Network (LAN)
- Wide Area Network (WAN)
- Ethernet switches and router applications

#### DESCRIPTION

ATGBICS QSFP-100G-ZR4-MSA-AT is a transceiver module designed for 80km optical communication applications. The design is compliant to 100GBASE-ZR4 of the IEEE 802.3-2012 Clause 88 standard IEEE 802.3bm CAUI-4 chip to module electrical standard ITU-T G.959.1-2012-02 standard . The module converts 4 inputs channels (ch) of 25.78 Gbps to 27.95Gbps electrical data to 4 lanes optical signals, and multiplexes them into a single channel for 100Gb/s optical transmission. Reversely, on the receiver side, the module

# Technical Datasheet

optically de-multiplexes a 100Gb/s input into 4 lanes signals, and converts them to 4 lanes output electrical data.

The central wavelengths of the 4 lanes are 1296 nm, 1300 nm, 1305 nm and 1309 nm . It contains a duplex LC connector for the optical interface and a 38-pin connector for the electrical interface. To minimize the optical dispersion in the long-haul system, single-mode fiber (SMF) has to be applied in this module.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP28 Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

The module operates from a single +3.3V power supply and LVCMOS/LVTTL global control signals such as Module Present, Reset, Interrupt and Low Power Mode are available with the modules. A 2-wire serial interface is available to send and receive more complex control signals and to obtain digital diagnostic information. Individual channels can be addressed and unused channels can be shut down for maximum design flexibility.

This product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP28 Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

## ABSOLUTE MAXIMUM RATINGS

The operation in excess of any absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	T <sub>o</sub>	-40	85	°C	
Relative Humidity(non-condensing)	RH	0	85	%	
Operating Case Temperature	T <sub>o</sub>	0	70	degC	
Supply Voltage	V <sub>ccT, R</sub>	-0.5	4	V	

## RECOMMENDED OPERATING CONDITIONS AND SUPPLY REQUIREMENTS

Parameter	Symbol	Min.	Typical	Max.	Unit
Case operating Temperature	TC	0		+70	°C
Supply Voltage	VCCT, R	+3.13	3.3	+3.47	V
Supply Current	ICC		1100	1500	mA
Power Dissipation	PD			5	W

# Technical Datasheet

## Electrical Characteristics (TOP = 0 to 70 °C, VCC = 3.13 to 3.47 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Data Rate per Channel		-	25.78125		Gbps	
			27.9525			
Power Consumption		-	3.6	5.5	W	
Supply Current	Icc		1.1	1.5	A	
Control I/O Voltage-High	VIH	2.0		Vcc	V	
Control I/O Voltage-Low	VIL	0		0.7	V	
Inter-Channel Skew	TSK			35	Ps	
RESETL Duration			10		Us	
RESETL De-assert time				100	ms	
Power On Time				100	ms	
Transmitter						
Single Ended Output Voltage Tolerance		0.3		Vcc	V	1
Common mode Voltage Tolerance		15			mV	
Transmit Input Diff Voltage	VI	150		1200	mV	
Transmit Input Diff Impedance	ZIN	85	100	115		
Data Dependent Input Jitter	DDJ		0.3		UI	
Receiver						
Single Ended Output Voltage Tolerance		0.3		4	V	
Rx Output Diff Voltage	Vo	370	600	950	mV	
Rx Output Rise and Fall Voltage	Tr/Tf			35	ps	1
Total Jitter	TJ		0.3		UI	

Note:

20 ~ 80%

# Technical Datasheet

## Optical Parameters(TOP = 0 to 70 °C, VCC = 3.0 to 3.6 Volts)

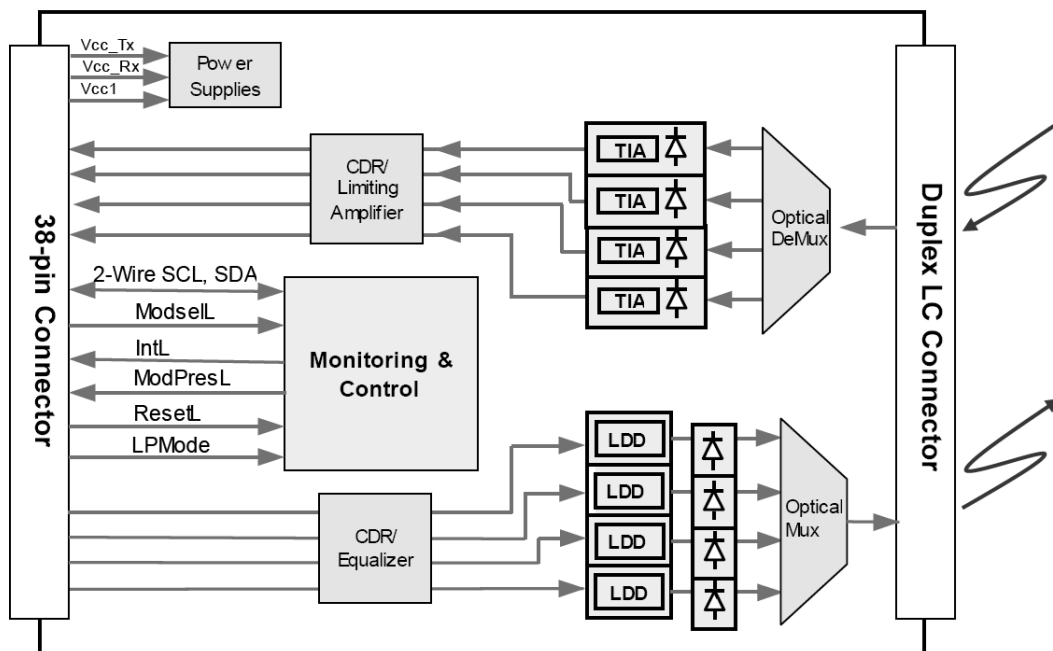
Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Transmitter						
Wavelength Assignment	L0	1294.53	1295.56	1296.59	nm	
	L1	1299.02	1300.05	1301.09	nm	
	L2	1303.54	1304.58	1305.63	nm	
	L3	1308.09	1309.14	1310.19	nm	
Side-mode Suppression Ratio	SMSR	30	-	-	dB	
Total Average Launch Power	PT	8.0	-	10.5	dBm	
Average Launch Power, each Lane		2.0	-	4.5	dBm	
Difference in Launch Power between any two Lanes (OMA)		-	-	6.5	dB	
Optical Modulation Amplitude, each Lane	OMA			3.5	dBm	
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane		-4.8	-		dBm	
TDP, each Lane	TDP			2.2	dB	
Extinction Ratio	ER	6.0	-	-	dB	
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				
Optical Return Loss Tolerance		-	-	20	dB	
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Relative Intensity Noise	Rin			-128	dB/HZ	1
Optical Return Loss Tolerance		-	-	12	dB	
Receiver						
Damage Threshold	THd	3.3			dBm	1
Average Power at Receiver Input, each Lane	R	-10.6		0	dBm	
RSSI Accuracy		-2		2	dB	
Receiver Reflectance	Rrx			-26	dB	
Receiver Power (OMA), each Lane		-	-	7	dBm	
LOS De-Assert	LOSD			-15	dBm	
LOS Assert	LOSA	-25			dBm	
LOS Hysteresis	LOSH	0.5			dB	

# Technical Datasheet

Note

12dB Reflection

## Transceiver Block Diagram



# Technical Datasheet

## PIN ASSIGNMENT

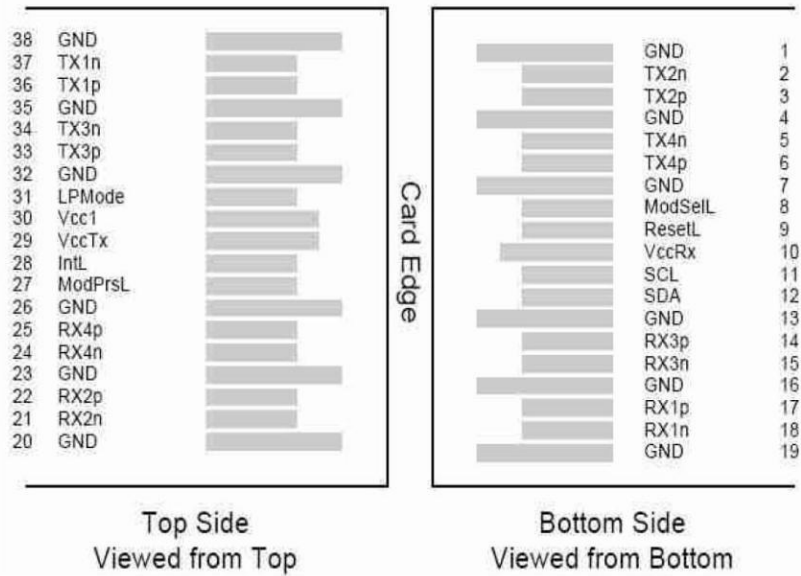


Diagram of Host Board Connector Block Pin Numbers and Name

## Pin Description

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Output	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Output	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVC MOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Inverted Data Output	

# Technical Datasheet

15	CML-O	Rx3n	Receiver Non-Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Inverted Data Output	
18	CML-O	Rx1n	Receiver Non-Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply Transmitter	2
30		Vcc1	+3.3V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Inverted Data Output	
34	CML-I	Tx3n	Transmitter Non-Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Inverted Data Output	
37	CML-I	Tx1n	Transmitter Non-Inverted Data Output	
38		GND	Ground	1

Notes:

GND is the symbol for single and supply(power) common for QSFP28 modules, All are common within the QSFP28 module and all module voltages are referenced to this potential otherwise noted. Connect these directly to the host board signal common ground plane. Laser output disabled on TDIS >2.0V or open, enabled on TDIS <0.8V.

VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. VccRx, Vcc1 and VccTx may be internally connected within the QSFP28 transceiver module in any combination. The connector pins are each rated for maximum current of 500mA.

# Technical Datasheet

## Mechanical Dimensions

