ATGBICS® by APPROVED TECHNOLOGY

Technical Datasheet

QSFP-40G-PLR4L-HW-C

Huawei® Compatible 40GBase-PLR4 QSFP+ Transceiver

Hot Pluggable, +3.3V, MTP/MPO, 1310nm, up to 1km, Commercial Temperature

FEATURES

- 4 CWDM lanes MUX/DEMUX design
- Up to 11.2Gbps per channel bandwidth
- Aggregate bandwidth of > 40Gbps
- Duplex LC connector
- Compliant with 40G Ethernet IEEE802.3ba and 40GBASE-PLR4 Standard
- QSFP MSA compliant
- Up to 1km transmission
- Compliant with QDR/DDR InfiniBand data rates
- Single +3.3V power supply operating
- Built-in digital diagnostic functions
- Commercial Operating Temperature Range: 0 to 70°C
- RoHS Compliant Part

APPLICATIONS

- Rack to rack
- Data centres Switches and Routers
- Metro networks
- Switches and Routers
- 40GBase-PLR4 Ethernet Links

Approved Technology Ltd. Wyncombe House, 2A Wyncombe Road, Southbourne, Dorset, BH5 2JU, United Kingdom
ATGBICS.com | Approved-Technology.com | +44 (0) 1202 424 518 | sales@approved-technology.com

ATGBICS® by APPROVED TECHNOLOGY

Technical Datasheet

DESCRIPTION

QSFP-40G-PLR4L-HW is a transceiver module designed for 1km optical communication applications. The design is compliant to 40GBase-PLR4 of the IEEE P802.3ba standard. The module converts 4 inputs channels (ch) of 10Gb/s electrical data to 4 CWDM optical signals and multiplexes them into a single channel for 40Gb/s optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 40Gb/s input into 4 CWDM channels signals and converts them to 4 channel output electrical data.

The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331nm as members of the CWDM wavelength grid defined in ITU-T G694.2. It contains a duplex LC connector for the optical interface and a 38-pin connector for the electrical interface. To minimize the optical dispersion in the long-haul system, single-mode fibre (SMF) must be applied in this module. The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

The module operates from a single +3.3V power supply and LVCMOS/LVTTL global control signals such as Module Present, Reset, Interrupt and Low Power Mode are available with the modules. A 2-wire serial interface is available to send and receive more complex control signals and to obtain digital diagnostic information. Individual channels can be addressed and unused channels can be shut down for maximum design flexibility.

The QSFP-40G-PLR4L-HW is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Temperature	T_O	0		70	°C
Storage Temperature	T_S	-40		85	°C
Supply Voltage	$V_{CC}T$, R	-0.5		4	V
Relative Humidity	RH	0		85	%

Recommended Operating Environment:

Parameter	Symbol	Min.	Typical	Max.	Unit
Case operating Temperature	T_O	0		70	°C
Supply Voltage	$V_{CCT, R}$	+3.13	3.3	+3.47	V
Supply Current	I_{CC}			1000	mA
Power Dissipation	PD			3.5	W

Approved Technology Ltd. Wyncombe House, 2A Wyncombe Road, Southbourne, Dorset, BH5 2JU, United Kingdom
ATGBICS.com | Approved-Technology.com | +44 (0) 1202 424 518 | sales@approved-technology.com

Technical Datasheet

Electrical Characteristics (T_O = 0 to 70 °C, VCC = 3.13 to 3.47 Volts

Parameter	Symbol	Min	Type	Max	Unit	Notes
Data Rate per Channel		-	10.3125	11.2	Gbps	
Power Consumption		-	2.5	3.5	W	
Supply Current	Icc		0.75	1.0	A	
Control I/O Voltage-High	VIH	2.0		Vcc	V	
Control I/O Voltage-Low	VIL	0		0.7	V	
Inter-Channel Skew	TSK			150	Ps	
RESETL Duration			10		Us	
RESETL De-assert time				100	ms	
Power On Time				100	ms	
Transmitter						
Single Ended Output Voltage Tolerance		0.3		4	V	1
Common mode Voltage Tolerance		15			mV	
Transmit Input Diff Voltage	VI	150		1200	mV	
Transmit Input Diff Impedance	ZIN	85	100	115		
Data Dependent Input Jitter	DDJ		0.3		UI	
Receiver						
Single Ended Output Voltage Tolerance		0.3		4	V	
Rx Output Diff Voltage	Vo	370	600	950	mV	
Rx Output Rise and Fall Voltage	Tr/Tf			35	ps	1
Total Jitter	TJ		0.3		UI	

Notes:

1. 20 ~ 80%

Approved Technology Ltd. Wyncombe House, 2A Wyncombe Road, Southbourne, Dorset, BH5 2JU, United Kingdom
ATGBICS.com | Approved-Technology.com | +44 (0) 1202 424 518 | sales@approved-technology.com

Technical Datasheet

Optical Parameters (T_O = 0 to 70 °C, Vcc = 3.0 to 3.6 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Transmitter						
Wavelength Assignment	L0	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5	nm	
	L2	1304.5	1311	1317.5	nm	
	L3	1324.5	1331	1337.5	nm	
Side-mode Suppression Ratio	SMSR	30	-	-	dB	
Total Average Launch Power	PT	-	-	8.3	dBm	
Average Launch Power, each Lane		-7	-	2.3	dBm	
Difference in Launch Power between any two Lanes (OMA)		-	-	6.5	dB	
Optical Modulation Amplitude, each Lane	OMA	-4		+3.5	dBm	
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane		-4.8	-		dBm	
TDP, each Lane	TDP			2.3	dB	
Extinction Ratio	ER	3.5	-	-	dB	
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				
Optical Return Loss Tolerance		-	-	20	dB	
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Relative Intensity Noise	Rin			-128	dB/HZ	1
Optical Return Loss Tolerance		-	-	12	dB	
Receiver						
Damage Threshold	THd	3.3			dBm	1
Average Power at Receiver Input, each Lane	R	-13.7		2.3	dBm	
Receiver Power (OMA), each Lane				3.5	dB	
Receive Electrical 3 dB upper Cut off Frequency, each Lane				12.3	GHz	
RSSI Accuracy		-2		2	dB	
Receiver Reflectance	Rrx			-26	dB	
Receiver Power (OMA), each Lane		-	-	3.5	dBm	
Stressed Receiver Sensitivity in OMA, each Lane		-	-	-9.9	dBm	
Receiver Sensitivity, each Lane	SR	-	-	-11.5	dBm	
Difference in Receive Power between any two Lanes (OMA)				7.5	dB	
Receive Electrical 3 dB upper Cutoff Frequency, each Lane				12.3	GHz	
LOS De-Assert	LOS_D			-15	dBm	
LOS Assert	LOS_A	-30			dBm	
LOS Hysteresis	LOS_H	0.5			dB	

Notes:

1. 12dB Reflection

Approved Technology Ltd. Wyncombe House, 2A Wyncombe Road, Southbourne, Dorset, BH5 2JU, United Kingdom
ATGBICS.com | Approved-Technology.com | +44 (0) 1202 424 518 | sales@approved-technology.com

Diagnostic Monitoring Interface

Digital diagnostics monitoring function is available on all QSFP+ PLR4. A 2-wire serial interface allows user to contact with module. The structure of the memory is shown in flowing. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses on the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function. The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

Approved Technology Ltd. Wyncombe House, 2A Wyncombe Road, Southbourne, Dorset, BH5 2JU, United Kingdom
ATGBICS.com | Approved-Technology.com | +44 (0) 1202 424 518 | sales@approved-technology.com

Timing for Soft Control and Status Functions

Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on1, hot plug or rising edge of Reset until the module is fully functional2
Reset Init Assert Time	t_reset_init	2	µs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin.
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on1 until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on1 to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional2
LPMode Assert Time	ton_LPMode	100	µs	Time from assertion of LPMode (Vin:LPMode =Vih) until module power consumption enters lower Power Level
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = Vol
IntL Deassert Time	toff_IntL	500	µs	toff_IntL 500 µs Time from clear on read3 operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted
Mask Assert Time	ton_mask	100	ms	Time from mask bit set4 until associated IntL assertion is inhibited
Mask De-assert Time	toff_mask	100	ms	Time from mask bit cleared4 until associated IntlL operation resumes
ModSelL Assert Time	ton_ModSelL	100	µs	Time from assertion of ModSelL until module responds to data transmission over the 2-wire serial bus
ModSelL Deassert Time	toff_ModSelL	100	µs	Time from deassertion of ModSelL until the module does not respond to data transmission over the 2-wire serial bus
Power_over-ride or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set 4 until module power consumption enters lower Power Level
Power over-ride or Power-set De-assert Time	toff_Pdown	300	ms	Time from P_Down bit cleared4 until the module is fully functional3

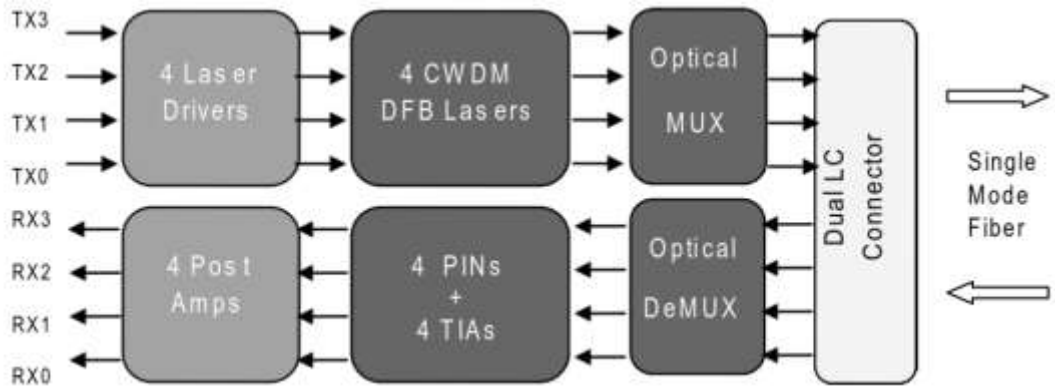
Notes:

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 de-asserted.
3. Measured from falling clock edge after stop bit of read transaction.
4. Measured from falling clock edge after stop bit of write transaction.

Approved Technology Ltd. Wyncombe House, 2A Wyncombe Road, Southbourne, Dorset, BH5 2JU, United Kingdom
ATGBICS.com | Approved-Technology.com | +44 (0) 1202 424 518 | sales@approved-technology.com

Technical Datasheet

Transceiver Block Diagram



Pin Assignment

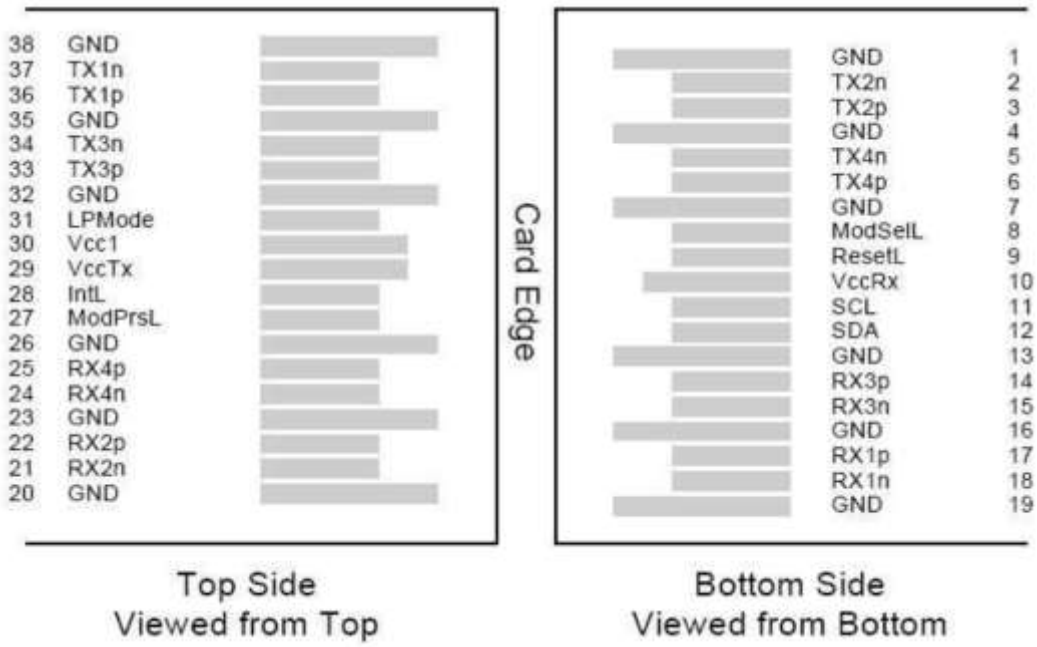


Diagram of Host Board Connector Block Pin Numbers and Name

Approved Technology Ltd. Wyncombe House, 2A Wyncombe Road, Southbourne, Dorset, BH5 2JU, United Kingdom
ATGBICS.com | Approved-Technology.com | +44 (0) 1202 424 518 | sales@approved-technology.com

Technical Datasheet

Pin Description

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Output	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Output	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Inverted Data Output	
15	CML-O	Rx3n	Receiver Non-Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Inverted Data Output	
18	CML-O	Rx1n	Receiver Non-Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply Transmitter	2
30		Vcc1	+3.3V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Inverted Data Output	
34	CML-I	Tx3n	Transmitter Non-Inverted Data Output	

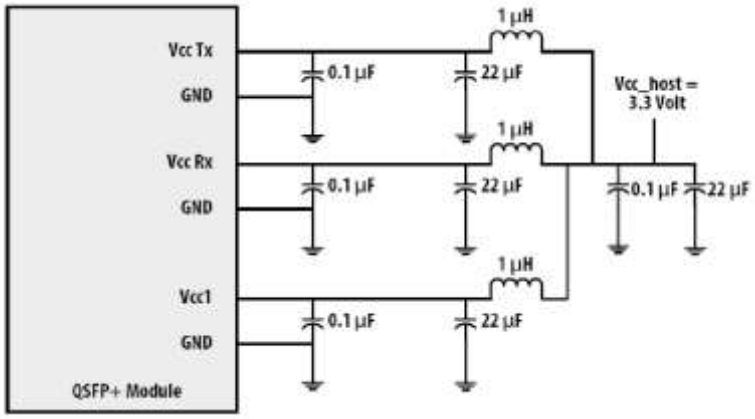
Approved Technology Ltd. Wyncombe House, 2A Wyncombe Road, Southbourne, Dorset, BH5 2JU, United Kingdom
ATGBICS.com | Approved-Technology.com | +44 (0) 1202 424 518 | sales@approved-technology.com

35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Inverted Data Output	
37	CML-I	Tx1n	Transmitter Non-Inverted Data Output	
38		GND	Ground	1

Notes:

1. GND is the symbol for single and supply(power) common for QSFP modules, all are common within the QSFP module, and all module voltages are referenced to this potential otherwise noted. Connect these directly to the host board signal common ground plane. Laser output disabled on TDIS >2.0V or open, enabled on TDIS <0.8V.
2. VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. VccRx, Vcc1 and VccTx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for maximum current of 500mA.

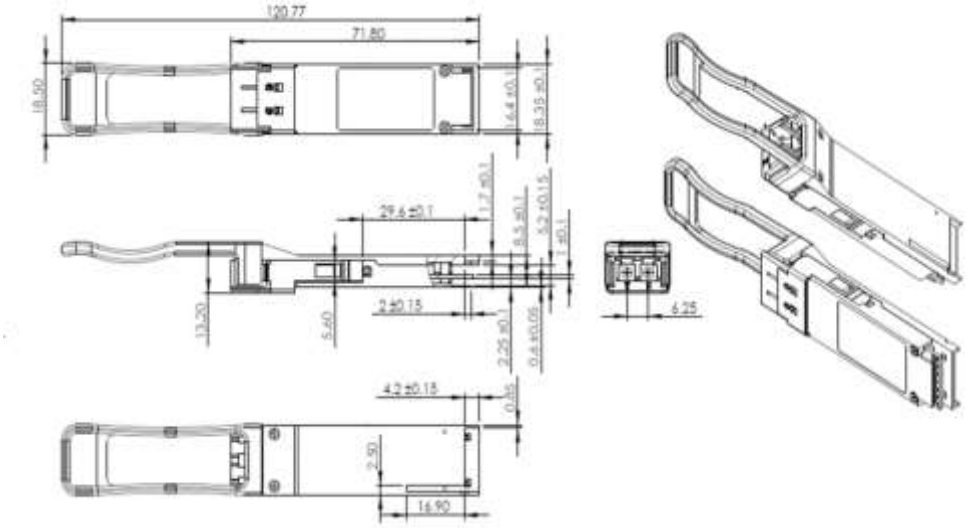
Recommended Circuit



Approved Technology Ltd. Wyncombe House, 2A Wyncombe Road, Southbourne, Dorset, BH5 2JU, United Kingdom
ATGBICS.com | Approved-Technology.com | +44 (0) 1202 424 518 | sales@approved-technology.com

Technical Datasheet

Mechanical Dimensions (units: mm)



Approved Technology Ltd. Wyncombe House, 2A Wyncombe Road, Southbourne, Dorset, BH5 2JU, United Kingdom
ATGBICS.com | Approved-Technology.com | +44 (0) 1202 424 518 | sales@approved-technology.com