ATGBICS® by APPROVED TECHNOLOGY

Technical Datasheet

QSFP-DD-400G-SR8

400GBase SR8 QSFP-DD Optical Transceiver

Hot Pluggable, +3.3V, MPO-16, 850nm, MMF, 100m, Commercial Temperature

FEATURES

- Hot-pluggable QSFP-DD form factor
- Maximum link length of 100m on OM4 fibre with FEC
- 8x50Gbps PAM4 modulation
- +3.3V single power supply
- Power dissipation < 9W
- Support DDM function
- MPO-16 APC connector
- RoHS compliant
- Commercial Operating Temperature Range: 0 to 70ºC

APPLICATIONS

- 400GBASE-SR8 Ethernet
- Telecom networking
- Data Centre Interconnect

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Storage Temperature	T_S	-40	-	85	ºC	
Supply Voltage	V_{CC}	-0.5	-	3.6	V	
Operating Humidity (No Condensation)	RH	5	-	85	%	
Receiver Damage Threshold per Lane	P_{RDMG}	5	-	-	dBm	

RECOMMENDED OPERATING ENVIRONMENT

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T_{OPR}	0	-	70	ºC	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Maximum Power Dissipation	P_D	-	-	9	W	
Transmission Distance	TD	-	-	100	m	1

Note:

1. 70m on OM3 fibre, 100m on OM4 fibre, with FEC.

ATGBICS.com | Approved-Technology.com | +44 (0) 1202 424 518 | sales@approved-technology.com

OPTICAL PARAMETERS

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
TRANSMITTER						
Data Rate, each lane		26.5625±100ppm			GBd	
Center Wavelength	λ_C	840	850	860	nm	
RMS Spectral width	$\Delta\lambda$	-	-	0.6	nm	
Average Launch Power, each lane		-6.5	-	4.0	dBm	
Outer Optical Modulation Amplitude (OMA_{outer}), each lane	T_{OMA}	-4.5	-	3	dBm	1
Launch Power in OMA_{outer} minus TDECQ, each lane	T_{OMA}	-5.9	-	-	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	-	-	4.5	dB	
Average Output Power (Laser Turn off)	T_{OFF}	-	-	-30	dBm	
Extinction Ratio, each lane	ER	3	-	-	dB	
Transmitter transition time, each lane	-	-	-	34	ps	
Optical Return Loss Tolerance	ORL	-	-	12	dB	
RECEIVER						
Data Rate, each lane		26.5625±100ppm			GBd	
Center Wavelength	λ_C	840	850	860	nm	
Damage Threshold, each lane	PIN	5	-	-	dBm	
Average Receive Power, each lane	AOP_R	-8.4	-	4.0	dBm	
Receive Power (OMA_{outer}), each lane	OMA_R	-	-	3	dBm	
Receiver Sensitivity (OMA_{outer}), each lane	S_{OMA}	-	-	max (-6.5, SECQ-7.9)	dBm	2
LOS Assert	LOSA	-30	-	-10	dBm	
LOS De-Assert	LOSD	-	-	-9	dBm	
LOS Hysteresis	LOSH	0.5	-	-	dB	

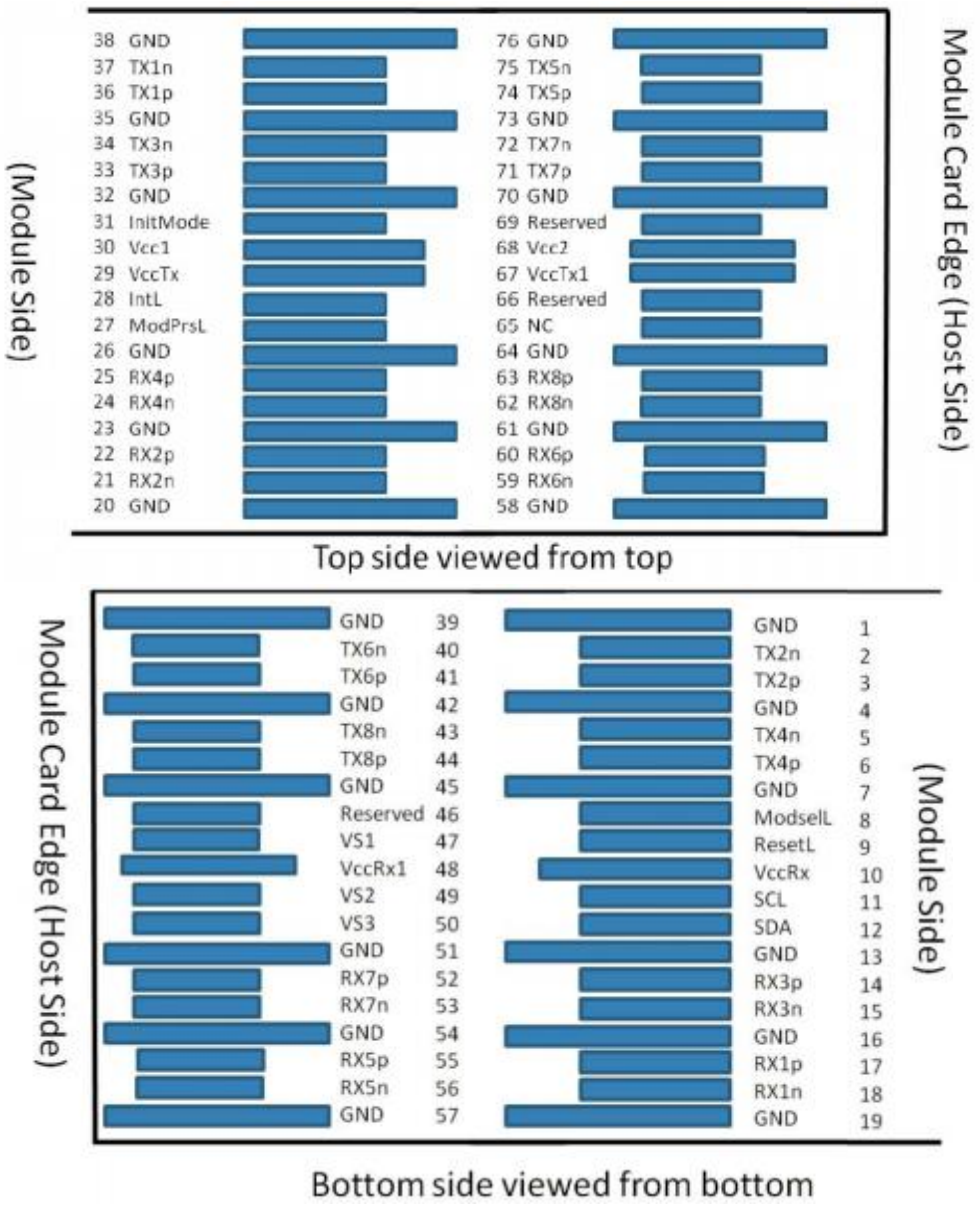
Note:

1. Even if the TDECQ < 1.4 dB, the OMAouter (min) must exceed this value
2. Bit Error Ratio < $2.4x10^{-4}$, Pattern PRBS31Q

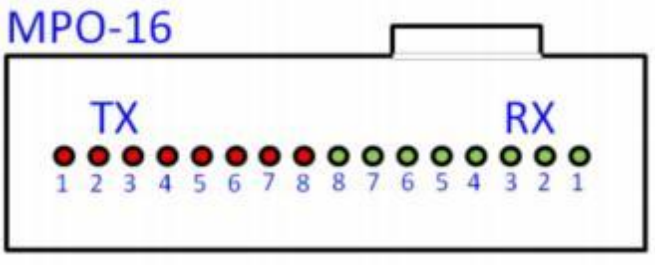
ELECTRICAL CHARACTERISTICS (High Speed Signal - Compliant with IEEE 802.3 400GAUI-8)

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
TRANSMITTER (Module Input, TP1)						
Signalling rate per lane		26.5625 ± 100 ppm			GBd	
Differential pk-pk input Voltage tolerance		900	-	-	mV	
Differential termination mismatch		-	-	10	%	
Single-ended voltage tolerance range		-0.4	-	3.3	V	
DC common mode Voltage		-350	-	2850	mV	
RECEIVER (Module Output, TP4)						
Signalling rate per lane		26.5625 ± 100 ppm			GBd	
Differential output Voltage		-	-	900	mV	
Near-end ESMW (Eye symmetry mask width)		0.265	-	-	UI	
Near-end Eye height, differential		70	-	-	mV	
Far-end ESMW (Eye symmetry mask width)		0.2	-	-	UI	
Far-end Eye height, differential		30	-	-	mV	
Differential Termination Mismatch		-	-	10	%	
Transition Time (min, 20% to 80%)		9.5	-	-	ps	
DC common mode Voltage		-350	-	2850	mV	

PIN ASSIGNMENT



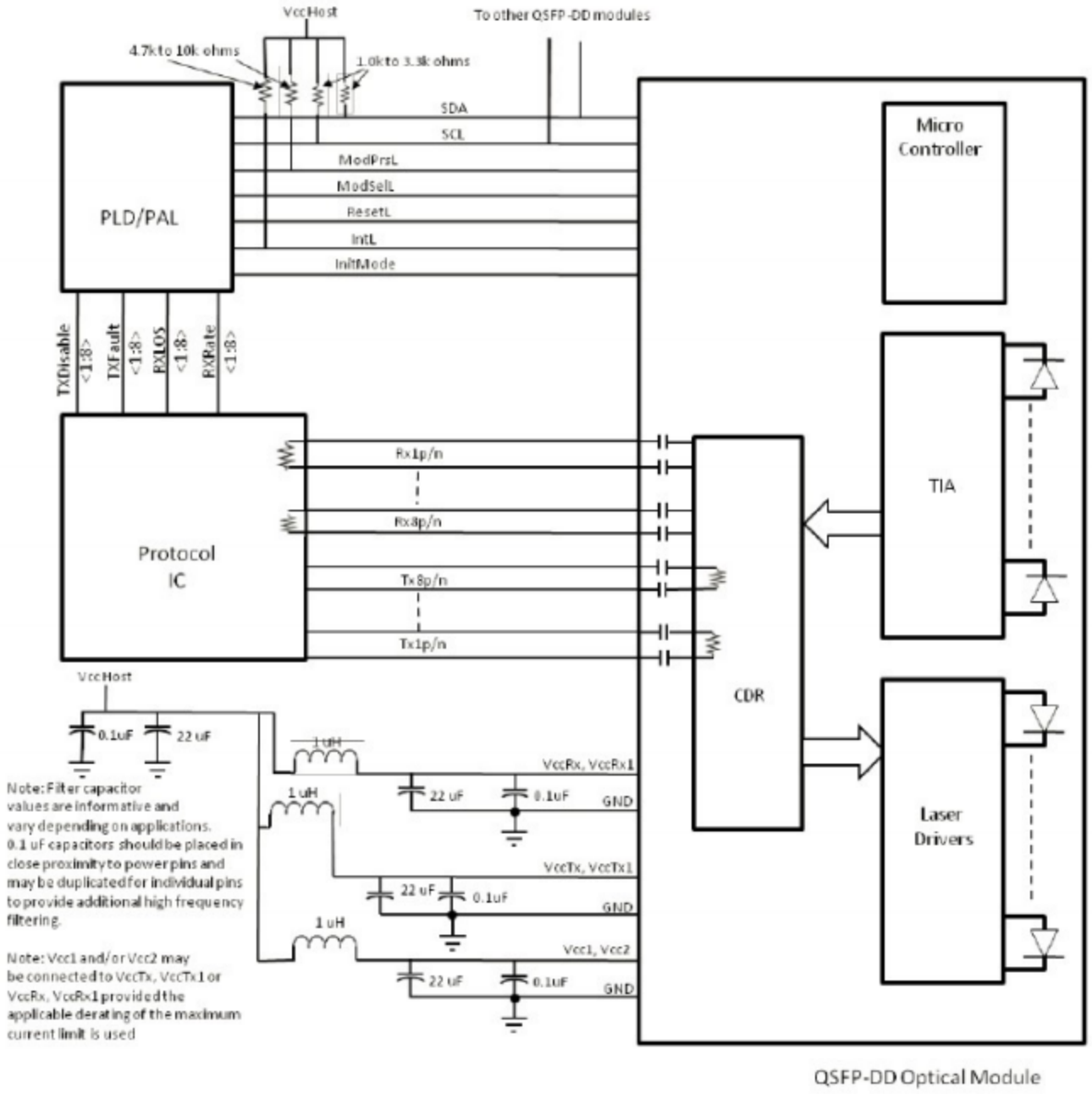
Pin definitions of the module high speed inputs/outputs



Active fibre ports in MPO-16 connector on module side

Pin	Logic	Symbol	Definition	Pin	Logic	Symbol	Definition
1		GND	Ground	**39**		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	**40**	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	**41**	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	**42**		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	**43**	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	**44**	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	**45**		GND	Ground
8	LVTTL-I	ModSelL	Module Select	**46**		Reserved	
9	LVTTL-I	ResetL	Module Reset	**47**		VS1	Module Vendor Specific 1
10		VccRx	+3.3V Power Supply Receiver	**48**		VccRx1	3.3V Power Supply
11	LVCMOS-I/O	SCL	2-wire serial interface clock	**49**		VS2	Module Vendor Specific 2
12	LVCMOS-I/O	SDA	2-wire serial interface data	**50**		VS3	Module Vendor Specific 3
13		GND	Ground	**51**		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	**52**	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	**53**	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	**54**		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	**55**	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	**56**	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	**57**		GND	Ground
20		GND	Ground	**58**		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	**59**	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	**60**	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	**61**		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output	**62**	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	**63**	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	**64**		GND	Ground
27	LVTTL-O	ModPrsL	Module Present	**65**		NC	Not connected
28	LVTTL-O	IntL	Interrupt	**66**		Reserved	
29		VccTx	+3.3V Power Supply Transmitter	**67**		VccTx1	3.3V Power Supply
30		Vcc1	+3.3V Power Supply	**68**		Vcc2	3.3V Power Supply
31	LVTTL-I	InitMode	Initialization mode	**69**		Reserved	
32		GND	Ground	**70**		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	**71**	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	**72**	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	**73**		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	**74**	CML-I	Tx5p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input	**75**	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	**76**		GND	Ground

RECOMMENDED HOST BOARD



Recommended QSFP-DD Host Board Schematic

MECHANICAL SPECIFICATIONS (UNIT: mm)