

Statement of Volatility – Dell PowerEdge R7615

Dell

PowerEdge R7615 contains both volatile and non-volatile (NV) components. Volatile components lose their data immediately upon removal of power from the component. Non-volatile components continue to retain their data even after the power has been removed from the component. Components chosen as user-definable configuration options (those not soldered to the motherboard) are not included in the Statement of Volatility. Configuration option information (pertinent to options such as microprocessors, remote access controllers, and storage controllers) is available by component separately. The following NV components are present in the PowerEdge R7615 server.

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|-----------------------|--------------------------|----------|----------------------|-----------|--------------------------------|---|---|-----------------------------------|-------------------------------------|---|
| Planar | | | | | | | | | | |
| CPU Internal CMOS RAM | Non-Volatile | 1 | CPU1 | 256 Bytes | Battery-backed CMOS RAM | No | Real-time clock and BIOS configuration settings | BIOS | N/A – BIOS only control | 1) Set NVRAM_CLR jumper to clear BIOS configuration settings at boot and reboot system. 2) Power off the system, remove coin cell battery for 30 seconds, replace battery and then power back on. 3) Restore default configuration in F2 system setup menu. |
| BIOS SPI Flash | Non-Volatile | 1 | U4103 | 32 MB | SPI Flash | No | Boot code, system configuration information, | SPI interface via CPU | Software write protected | Not possible with any utilities or applications and system is not functional if corrupted or |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---------------------|--------------------------|----------|----------------------|------|--------------------------------|---|---|-----------------------------------|--|---|
| | | | | | | | UEFI environment | | | removed. |
| BIOS Data SPI Flash | Non-Volatile | 1 | U19 | 4 MB | SPI Flash | No | 4MB Data SPI ROM storage BIOS setting. | SPI interface via CPU | Software write protected | Not possible with any utilities or applications and the system is not functional if BIOS SPI is corrupted or removed. |
| iDRAC SPI Flash | Non-Volatile | 1 | U29 | 4 MB | SPI Flash | No | iDRAC Uboot (boot loader), server management persistent store (i.e. iDRAC boot variables), and virtual planar FRU | SPI interface via iDRAC | Embedded iDRAC subsystem firmware actively controls sub area based write protection as needed. | The user cannot clear memory completely. However, user data, lifecycle log and archive, SEL, and firmware image repository can be cleared using Delete Configuration and Retire System, which can be accessed through the Lifecycle Controller interface. |
| BMC EMMC | Non-Volatile | 1 | U4101 | 8 GB | eMMC NAND Flash | No | Operational iDRAC FW, Lifecycle Controller (LC) USC partition, LC service diags, LC | NAND Flash interface via iDRAC | Embedded FW write protected | The user cannot clear memory completely. However, user data, lifecycle log and archive, SEL, and firmware image repository can be cleared |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|------------------------------------|--------------------------|----------|-----------------------|----------------------|--------------------------------|---|--|--|--|---|
| | | | | | | | OS drivers, USC firmware, iDRAC MAC Address, and EPPID, rac log, System Event Log, lifecycle log cache | | | using Delete Configuration and Retire System, which can be accessed through the Lifecycle Controller interface. |
| iDRAC DDR4 | Volatile | 1 | U_IDRAC9_DRAM1 | 8Gb | RAM | Yes | iDRAC RAM | iDRAC firmware | Not write-protected | Remove AC |
| System CPLD RAM | Volatile | 1 | U_CPLD1 | 432 kb | RAM | No | Not utilized | Not utilized | Not accessible | Not accessible |
| System CPLD Flash | Non-Volatile | 1 | U_CPLD1 | 448 kb | FLASH | No | Power on System Firmware | Firmware update | BIOS Security Protocols | Not user clearable |
| System Memory: RDIMM | Volatile | Up to 12 | CPU1: A1~A12 | Up to 256GB per DIMM | RAM | Yes | System OS RAM | System OS | OS Control | Reboot or power down system |
| CPU_VDDCR_CORE0,, CPU_VDDCR_CORE1, | Non-Volatile | 3 | CPU1: U50, U128,U123, | 64KB | OTP (one time programmable) | No | Operational parameters | Once values are loaded into register space a cmd writes to nvme. | There are passwords for different sections of the register space | The user cannot clear memory. |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---------------------|--------------------------|----------|----------------------|------|--------------------------------|---|---------------------------|-----------------------------------|-------------------------------------|----------------------------|
| VDDIO IO Controller | | | | | | | | | | |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|--------------------------------------|--------------------------|----------|----------------------|--------------------------------|--------------------------------|---|---------------------------|--------------------------------------|-------------------------------------|-------------------------------|
| 8x3.5" SAS3/SATA BP (5TP8Y) | | | | | | | | | | |
| SEP internal flash | Non-Volatile | 1 | U46 | 4Mbit in-chip SPI Serial Flash | Integrated Flash+EEPROM | No | Firmware + FRU | I2C interface via iDRAC | Program write protect bit | The user cannot clear memory. |
| Backplane External FRU | Non-Volatile | 1 | U46 | 256 Bytes | I2C EEPROM | No | FRU | Programmed at ICT during production. | No write protected | The user cannot clear memory. |
| 12 x3.5" SAS3/SATA BP (T158T) | | | | | | | | | | |

| | | | | | | | | | | |
|--|------------------------------|---|---------|--------------------------------|-------------------------|----|----------------|--------------------------------------|---------------------------|-------------------------------|
| SEP internal flash | Non-Volatile | 1 | U16 | 4Mbit in-chip SPI Serial Flash | Integrated Flash+EEPROM | No | Firmware + FRU | I2C interface via iDRAC | Program write protect bit | The user cannot clear memory. |
| Backplane External FRU | Non-Volatile | 1 | U16 | 256 Bytes | I2C EEPROM | No | FRU | Programmed at ICT during production. | No write protected | The user cannot clear memory. |
| 8x2.5" Uni BP (YD2C2) | | | | | | | | | | |
| SEP internal flash | Non-Volatile | 1 | U14 | 4Mbit in-chip SPI Serial Flash | Integrated Flash+EEPROM | No | Firmware + FRU | I2C interface via iDRAC | Program write protect bit | The user cannot clear memory. |
| Backplane External FRU | Non-Volatile | 1 | U14 | 256 Bytes | I2C EEPROM | No | FRU | Programmed at ICT during production. | No write protected | The user cannot clear memory. |
| 8x2.5" SAS4/SATA v2 BP (XR5G5) | | | | | | | | | | |
| SEP internal flash | Non-Volatile Non-Volatile | 1 | U46 | 4Mbit in-chip SPI Serial Flash | Flash | No | Firmware + FRU | I2C interface via iDRAC | Program write protect bit | The user cannot clear memory. |
| Backplane External FRU | | | | 256 Bytes | | No | FRU | Programmed at ICT during production | No write protected | |
| 24x2.5" SAS4/SATA expander Backplane(GRT5N) | | | | | | | | | | |
| SEP internal flash | Non-Volatile | 2 | U14,U15 | 4Mbit in-chip SPI Serial Flash | Integrated Flash+EEPROM | No | Firmware + FRU | I2C interface via iDRAC | Program write protect bit | The user cannot clear memory. |

| | | | | | | | | | | |
|--------------------------------------|--------------|---|------------|--------------------------------|-------------------------|----|--------------------|--------------------------------------|---------------------------|-------------------------------|
| Expander Fru | Non-Volatile | 1 | U3 | 256Kb | EEPROM | No | Expander FRU | Programmed at ICT during production. | No write protected | The user cannot clear memory. |
| Expander Flash | Non-Volatile | 1 | U_FLASH1 | 128Mb | SPI Flash | No | Card firmware | I2C interface via iDRAC | Program write protect bit | The user cannot clear memory. |
| Expander NVSRAM | Non-Volatile | 1 | U_NVSRAM 1 | 128KB | NVSRAM | No | Configuration data | I2C interface via iDRAC | Program write protect bit | The user cannot clear memory. |
| Rear 2x2.5" univ SAS4 (X6XG3) | | | | | | | | | | |
| SEP internal flash | Non-Volatile | 1 | U47 | 4Mbit in-chip SPI Serial Flash | Integrated Flash+EEPROM | No | Firmware + FRU | I2C interface via iDRAC | Program write protect bit | The user cannot clear memory. |
| Backplane External FRU | Non-Volatile | 1 | U47 | 256 Bytes | I2C EEPROM | No | FRU | Programmed at ICT during production. | No write protected | The user cannot clear memory. |
| Rear 4x2.5" univ SAS4 (69NN3) | | | | | | | | | | |
| SEP internal flash | Non-Volatile | 1 | U47 | 4Mbit in-chip SPI Serial Flash | Integrated Flash+EEPROM | No | Firmware + FRU | I2C interface via iDRAC | Program write protect bit | The user cannot clear memory. |

| | | | | | | | | | | |
|--|------------------|---|-----|-----------|------------|----|--------------------------------------|--|---|----------------------------------|
| Backplane External FRU | Non- Volatile | 1 | U47 | 256 Bytes | I2C EEPROM | No | FRU | Programmed at ICT during production. | No write protected | The user cannot clear memory. |
| 4x E3 G5x2 Rear Ortho(62W2P) | | | | | | | | | | |
| | | | | | | | | | | |
| | | | | | | | | | | |
| 2U 24x2.5" NVMe Switch BP - Atlas 2 Gen5 (3TMCM) | | | | | | | | | | |
| | | | | | | | | | | |
| | | | | | | | | | | |
| 2U 8x E3 G5x2 G5x4 Ortho(32M85) | | | | | | | | | | |
| | | | | | | | | | | |
| | | | | | | | | | | |
| HBA355i fPERC (Internal controller)(T761Y) | | | | | | | | | | |
| SPI Flash | Non- Volatile | 1 | U2 | 128Mb | SPI Flash | No | Card firmware | Pre- programmed before assembly. Can be updated using Dell/LSI tools | Not write protected. Not visible to Host Processor | User cannot clear the memory. |
| FRU | Non- volatile | 1 | U5 | 2Kb | EEPROM | No | Card manufacturing information | Programmed at ICT during production. | Not write protected | User cannot clear the memory. |

| | | | | | | | | | | |
|--|--------------|---|-----|-------|-----------|----|--|---|--|-------------------------------|
| CPLD | Non-volatile | 1 | U23 | 24kb | Flash | No | Power sequencing and Cache Offload | Controller may program data during FW update | Not write protected Not visible to host CPU | User cannot clear this memory |
| MCU (Cordoba) | Non-volatile | 1 | U41 | 8kB | EEPROM | No | PCIe Bifurcation information to system iDRAC | BMC may program data if there is an updated version packaged with iDRAC | Not write protected Not visible to host CPU | User cannot clear this memory |
| H355,FPERC (Internal controller)(TKK9K) | | | | | | | | | | |
| SPI Flash | Non-Volatile | 1 | U2 | 128Mb | SPI Flash | No | Card firmware | Pre-programmed before assembly. Can be updated using Dell/LSI tools | Not write protected. Not visible to Host Processor | User cannot clear the memory. |
| FRU | Non-volatile | 1 | U5 | 2Kb | EEPROM | No | Card manufacturing information | Programmed at ICT during production. | Not write protected | User cannot clear the memory. |
| CPLD | Non-volatile | 1 | U23 | 24kb | Flash | No | Power sequencing and Cache Offload | Controller may program data during FW update | Not write protected Not visible to host CPU | User cannot clear this memory |
| MCU (Cordoba) | Non-volatile | 1 | U41 | 8kB | EEPROM | No | PCIe Bifurcation information to system iDRAC | BMC may program data if there is an updated version packaged with | Not write protected Not visible to host CPU | User cannot clear this memory |

| | | | | | | | | | | |
|---|--------------|---|-----|-------|-------------------------|----|------------------------------------|---|--|-------------------------------|
| | | | | | | | | iDRAC | | |
| NVSRAM | Non-volatile | 1 | U3 | 128kB | NVSRAM | No | Configuration data | ROC writes configuration data to NVSRAM | Not write protected Not visible to host CPU | User cannot clear this memory |
| H355,ADPT (Internal controller)(VCV6T) | | | | | | | | | | |
| SPI Flash | Non-Volatile | 1 | U2 | 128Mb | SPI Flash | No | Firmware | Pre-programmed before assembly. Can be updated using Dell/LSI tools | no write protected. Not visible to Host Processor | User can clear the memory. |
| FRU | Non-volatile | 1 | U5 | 2Kb | EEPROM | No | Card manufacturing information | Programmed at ICT during production. | no write protected | User cannot clear the memory. |
| CPLD | Non-volatile | 1 | U23 | 24kb | Integrated Flash+EEPROM | No | Power sequencing and Cache Offload | Pre-programmed before assembly. Can be updated using Dell/LSI tools | no write protected. Not visible to Host Processor | User cannot clear the memory. |
| HBA465E,ADPT (External controller)(8Y0MW) | | | | | | | | | | |
| SPI Flash | Non-Volatile | 1 | U2 | 128Mb | SPI Flash | No | Firmware | Pre-programmed before assembly. Can be updated using Dell/LSI tools | no write protected. Not visible to Host Processor | User can clear the memory. |
| FRU | Non- | 1 | U5 | 2Kb | EEPROM | No | Card | Programmed | no write protected | User cannot clear the |

| | | | | | | | | | | |
|--|--------------|---|-------------|-------|-------------------------|----|------------------------------------|---|---|---|
| | volatile | | | | | | manufacturing information | at ICT during production. | | memory. |
| CPLD | Non-volatile | 1 | U23 | 24kb | Integrated Flash+EEPROM | No | Power sequencing and Cache Offload | Pre-programmed before assembly. Can be updated using Dell/LSI tools | no write protected. Not visible to Host Processor | User cannot clear the memory. |
| H755 PERC (Internal Controller)(3KDWX) | | | | | | | | | | |
| SDRAM | Volatile | 9 | U1077~U1085 | 8GB | SDRAM | No | Cache for HDD I/O | ROC writes to this memory - using it as cache for data IO to HDDs | no write protected. Not visible to Host Processor | Cache can be cleared by powering off the card |
| ONFI | Non-volatile | 1 | U1100 | 512Gb | NAND Flash | No | | ROC backs up DDR data to this device in case of a power failure | no write protected. Not visible to Host Processor | User cannot clear the memory. |
| BMU | Non-Volatile | 1 | U1126 | 180KB | Integrated Flash+EEPROM | No | Battery Management control | Programmed at ICT during production | no write protected. Not visible to Host Processor | User cannot clear the memory. |
| SPI Flash | Non-Volatile | 1 | U1086 | 128Mb | SPI Flash | No | Holds cache data during power loss | Pre-programmed before assembly. Can be updated using Dell/LSI tools | no write protected. Not visible to Host Processor | User can clear the memory. |
| NVSRAM | Non-volatile | 1 | U1087 | 128KB | NVSRAM | No | Configuration data | ROC writes configuration data to NVSRAM | no write protected. Not visible to Host Processor | |

| | | | | | | | | | | |
|---|--------------|---|-------|-------|--------|----|--|---|---|-------------------------------|
| FRU | Non-volatile | 1 | U1019 | 2Kb | EEPROM | No | Card manufacturing information | Programmed at ICT during production. | no write protected | User cannot clear the memory. |
| SPD | Non-volatile | 1 | U22 | 2Kb | EEPROM | No | Memory configuration data | Programmed at ICT during production. ROC read the configured data from the SPD for DDR settings | no write protected. Not visible to Host Processor | User cannot clear the memory. |
| CPLD | Non-volatile | 1 | U1088 | 64kb | Flash | No | Power sequencing and Cache Offload | Pre-programmed before assembly. Can be updated using Dell/LSI tools | no write protected. Not visible to Host Processor | User cannot clear the memory. |
| MCU (Cordova) | Non-volatile | 1 | U41 | 8KB | EEPROM | No | PCIe Bifurcation information to system iDRAC | Pre-programmed before assembly. Can be updated using Dell/LSI tools | no write protected. Not visible to Host Processor | User cannot clear the memory. |
| H755N PERC (Internal Controller) (9K2C2) | | | | | | | | | | |
| NVSRAM | Non-volatile | 1 | U1087 | 128KB | NVSRAM | No | Configuration data | ROC writes configuration data to NVSRAM | No write protected. Not visible to Host Processor | User cannot clear the memory. |
| FRU | Non-volatile | 1 | U1019 | 2Kb | EEPROM | No | Card manufacturing information | Programmed at ICT during production. | No write protected | User cannot clear the memory. |

| | | | | | | | | | | |
|---------------|--------------|---|-------------|-------|-----------|----|--|---|---|--|
| SPD | Non-volatile | 1 | U1019 | 2Kb | EEPROM | No | Memory configuration data | Pre-programmed before assembly | No write protected. Not visible to Host Processor | User cannot clear the memory. |
| NV Flash | Non-volatile | 1 | U1100 | 512Gb | SPI Flash | No | Card firmware | Pre-programmed before assembly. Can be updated using Dell/LSI tools | No write protected. Not visible to Host Processor | User cannot clear the memory. |
| CPLD | Non-volatile | 1 | U1088 | 64kb | Flash | No | Power sequencing and Cache Offload | NA | NA | NA |
| SPI Flash | Non-Volatile | 1 | U1086 | 128Mb | SPI Flash | No | Holds cache data during power loss | FPGA backs up DDR data to this device in case of a power failure | No write protected. Not visible to Host Processor | Flash can be cleared by powering up the card and allowing the controller to flush the contents to VD's. If the VD's are no longer available, cache can be cleared by going into controller BIOS and selecting Discard Preserved Cache. |
| SDRAM | Volatile | 9 | U1077~U1085 | 8GB | SDRAM | No | Cache for HDD I/O | ROC writes to this memory - using it as cache for data IO to HDDs | No write protected. Not visible to Host Processor | Cache can be cleared by powering off the card |
| MCU (Cordoba) | Non-volatile | 1 | U41 | 8KB | EEPROM | No | PCIe Bifurcation information to system iDRAC | NA | NA | NA |
| BMU | Non-Volatile | 1 | U1126 | 180KB | NA | No | Battery Management control | NA | NA | NA |

| H755 ADPT PERC (Internal Controller) (29XMF) | | | | | | | | | | |
|--|--------------|---|-------------|-------|---------------------------|----|------------------------------------|---|---|--|
| SDRAM | Volatile | 9 | U1077~U1085 | 8GB | SDRAM | No | Cache for HDD I/O | ROC writes to this memory - using it as cache for data IO to HDDs | no write protected. Not visible to Host Processor | Cache can be cleared by powering off the card |
| NV Flash | Non-volatile | 1 | U1100 | 512Gb | SPI Flash | No | Card firmware | Pre-programmed before assembly. Can be updated using Dell/LSI tools | no write protected. Not visible to Host Processor | User cannot clear the memory. |
| BMU | Non-Volatile | 1 | U1126 | 180KB | Integrated Flash + EEPROM | No | Battery Management Control | ROC may program data during FW and during boot during battery detection | Not write protected Not visible to host CPU | User cannot clear this memory |
| SPI Flash | Non-Volatile | 1 | U1086 | 128Mb | SPI Flash | No | Holds cache data during power loss | FPGA backs up DDR data to this device in case of a power failure | no write protected. Not visible to Host Processor | Flash can be cleared by powering up the card and allowing the controller to flush the contents to VD's. If the VD's are no longer available, cache can be cleared by going into controller BIOS and selecting Discard Preserved Cache. |
| NVSRAM | Non-volatile | 1 | U1087 | 128KB | NVSRAM | No | Configuration data | ROC writes configuration data to NVSRAM | no write protected. Not visible to Host Processor | User cannot clear the memory. |

| | | | | | | | | | | |
|--|--------------|---|-------|-------|-----------|----|--|--|--|-------------------------------|
| FRU | Non-volatile | 1 | U1019 | 2Kb | EEPROM | No | Card manufacturing information | Programmed at ICT during production. | no write protected | User cannot clear the memory. |
| SPD | Non-volatile | 1 | U22 | 2Kb | EEPROM | No | Memory configuration data | Pre-programmed before assembly | no write protected. Not visible to Host Processor | User cannot clear the memory. |
| CPLD | Non-volatile | 1 | U1088 | 64kb | Flash | No | Power sequencing and Cache Offload | ROC may program data during FW update | Not write protected Not visible to host CPU | User cannot clear this memory |
| H965i FPERC (Internal Controller) (NG8NP) | | | | | | | | | | |
| SPI Flash | Non-Volatile | 1 | U2 | 256Mb | SPI Flash | No | Card firmware | Pre-programmed before assembly. Can be updated using Dell/Broadcom tools | Not write protected. Not visible to Host Processor | User cannot clear the memory. |
| FRU | Non-volatile | 1 | U1019 | 2Kb | EEPROM | No | Card manufacturing information | Programmed at ICT during production. | Not write protected | User cannot clear the memory. |
| CPLD | Non-volatile | 1 | U1088 | 64kb | Flash | No | Power sequencing and Cache Offload | Controller may program data during FW update | Not write protected Not visible to host CPU | User cannot clear this memory |
| MCU (Cordoba) | Non-volatile | 1 | U41 | 8kB | Flash | No | PCIe Bifurcation information to system iDRAC | BMC may program data if there is an updated version packaged with | Not write protected Not visible to host CPU | User cannot clear this memory |

| | | | | | | | | | | |
|--|--------------|---|-------------|-------|---------------------------|----|--|---|--|---|
| | | | | | | | | iDRAC | | |
| NVSRAM | Non-volatile | 1 | U1087 | 128kB | NVSRAM | No | Configuration data | ROC writes configuration data to NVSRAM | Not write protected Not visible to host CPU | User cannot clear this memory |
| BMU | Non-Volatile | 1 | U1126 | 180KB | Integrated Flash + EEPROM | No | Battery Management control | ROC may program data during FW and during boot | Not write protected | User cannot clear this memory |
| SPD | Non-volatile | 1 | U22 | 256b | EEPROM | No | Memory configuration data | Pre-programmed before assembly | No write protected. Not visible to Host Processor | User cannot clear the memory. |
| NAND Flash | Non-volatile | 1 | U1100 | 512Gb | ONFI Flash | No | Cache offload during unexpected power loss | Programmed by ROC during cache offload | No write protected. Not visible to Host Processor | User cannot clear the memory. |
| SDRAM | Volatile | 9 | U1077~U1086 | 8GB | SDRAM | No | Cache for HDD I/O | ROC writes to this memory - using it as cache for data IO to HDDs | No write protected. Not visible to Host Processor | Cache can be cleared by powering off the card |
| H965e PERC (External Controller) (VWHMH) | | | | | | | | | | |
| SDRAM | Volatile | 9 | U1077~U1085 | 8GB | SDRAM | No | Cache for HDD I/O | ROC writes to this memory - using it as cache for data IO to HDDs | no write protected. Not visible to Host Processor | Cache can be cleared by powering off the card |
| ONFI | Non-volatile | 1 | U1100 | 512Gb | ONFI Nand | No | Memory backup storage for DDR4 | ROC backs up DDR data to this device in case of a | no write protected. Not visible to Host Processor | User cannot clear the memory. |

| | | | | | | | | | | |
|---------------|--------------|---|-------|-------|-------------------------|----|------------------------------------|---|---|-------------------------------|
| | | | | | | | | power failure | | |
| BMU | Non-Volatile | 1 | U1126 | 180KB | Integrated Flash+EEPROM | No | Battery Management control | Programmed at ICT during production | no write protected. Not visible to Host Processor | User cannot clear the memory. |
| SPI Flash | Non-Volatile | 1 | U2 | 128Mb | SPI Flash | No | Firmware | Pre-programmed before assembly. Can be updated using Dell/LSI tools | no write protected. Not visible to Host Processor | User can clear the memory. |
| NVSRAM | Non-volatile | 1 | U1087 | 128KB | Flash | No | Power sequencing and Cache Offload | ROC writes configuration data to NVSRAM | no write protected. Not visible to Host Processor | User cannot clear the memory. |
| FRU | Non-volatile | 1 | U1019 | 2Kb | EEPROM | No | Board manufacture information | Programmed at ICT during production. | no write protected | User cannot clear the memory. |
| SPD | Non-volatile | 1 | U22 | 2Kb | EEPROM | No | Memory configuration information | Pre-programmed before assembly | no write protected. Not visible to Host Processor | User cannot clear the memory. |
| CPLD | Non-volatile | 1 | U1088 | 64kb | Integrated Flash+EEPROM | No | Power sequencing and Cache Offload | Pre-programmed before assembly. Can be updated using Dell/LSI tools | no write protected. Not visible to Host Processor | User cannot clear the memory. |
| MCU (Cordova) | Non-volatile | 1 | U41 | 8KB | Integrated Flash+EEPROM | No | Battery Management control | Pre-programmed before assembly. Can | no write protected. Not visible to Host Processor | User cannot clear the memory. |

| | | | | | | | | | | |
|---|--------------|---|-------|-------|---------------------------|----|------------------------------------|---|--|-------------------------------|
| | | | | | | | | be updated using Dell/LSI tools | | |
| H965I ADPT PERC(External Controller) (W3T2J) | | | | | | | | | | |
| SPI Flash | Non-Volatile | 1 | U2 | 256Mb | SPI Flash | No | Card firmware | Pre-programmed before assembly. Can be updated using Dell/LSI tools | Not write protected. Not visible to Host Processor | User cannot clear the memory. |
| FRU | Non-volatile | 1 | U1019 | 2Kb | EEPROM | No | Card manufacturing information | Programmed at ICT during production. | Not write protected | User cannot clear the memory. |
| CPLD | Non-volatile | 1 | U1088 | 24kb | Flash | No | Power sequencing and Cache Offload | Controller may program data during FW update | Not write protected Not visible to host CPU | User cannot clear this memory |
| BMU | Non-Volatile | 1 | U1126 | 180KB | Integrated Flash + EEPROM | No | Battery Management control | ROC may program data during FW and during boot | Not write protected | User cannot clear this memory |
| NVSRAM | Non-volatile | 1 | U1087 | 128kB | NVSRAM | No | Configuration data | ROC writes configuration data to NVSRAM | Not write protected Not visible to host CPU | User cannot clear this memory |
| SPD | Non-volatile | 1 | U22 | 256b | EEPROM | No | Memory configuration data | Pre-programmed before assembly | No write protected. Not visible to Host Processor | User cannot clear the memory. |
| NAND Flash | Non-volatile | 1 | U1100 | 512Gb | ONFI Flash | No | Cache offload during | Programmed by ROC during cache offload | No write protected. Not | User cannot clear the memory. |

| | | | | | | | | | | |
|-------|----------|---|-------------|-----|-------|----|-----------------------|---|---|---|
| | | | | | | | unexpected power loss | | visible to Host Processor | |
| SDRAM | Volatile | 9 | U1077~U1086 | 8GB | SDRAM | No | Cache for HDD I/O | ROC writes to this memory - using it as cache for data IO to HDDs | No write protected. Not visible to Host Processor | Cache can be cleared by powering off the card |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|-----------------------------------|--------------------------|----------|----------------------|-------|--------------------------------|---|--|--|--|-------------------------------|
| Status LED Control Panel | | | | | | | | | | |
| Microcontroller | Non-Volatile | 1 | U_TINY | 8KB | Flash | No | Driving Health and Status LED | I2C via iDRAC | Hardware strapping | User cannot clear the memory. |
| Standard/LC RIO | | | | | | | | | | |
| MCU | Non-Volatile | 1 | U6 | 8kB | Flash ROM | No | Standard /LC RIO information | The data is flash via iDRAC auto update | No write protected. Not visible to Host Processor | User cannot clear the memory. |
| Power Button Control Panel | | | | | | | | | | |
| SPI Flash | Non-Volatile | 1 | U2 | 32 Mb | SPI Flash | No | EasyRestore functionality contains Service Tag, Copy of SEL logs | SPI interface from iDRAC to Right Cntl Panel | Embedded iDRAC subsystem firmware actively controls sub area based write protection as needed. | The user cannot clear memory. |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|------------|--------------------------|----------|----------------------|---|--------------------------------|---|------------------------------|---|--|-------------------------------|
| LOM | | | | | | | | | | |
| SPI Flash | Non-Volatile | 1 | U1 | 8-Mbit DataFlash (with Extra 256-Kbits) | SPI Flash EEPROM | Yes | Firmware, configuration data | Firmware and some configuration data flashed via Dell Update Package (DUP); some configuration data is programmed during manufacturing; end user configuration data is written via UEFI HII | Reserving write protection function for HW design. | User cannot clear the memory. |
| MCU | Non-Volatile | 1 | U2 | 64KB Flash and 8KB of SRAM | Flash ROM | No | LOM Security data | Off-line programming Before production | No write protected. Not visible to Host Processor | User cannot clear the memory |
| TPM | | | | | | | | | | |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|-------------------------------|--------------------------|----------|----------------------|-----------|--------------------------------|---|--------------------------------|---|-------------------------------------|-------------------------------|
| Trusted Platform Module (TPM) | Non-Volatile | 1 | U2 | 128 Bytes | EEPROM | Yes | Storage of encryption keys | Using TPM Enabled operating systems | SW write protected | F2 Setup option |
| BOSS N1 | | | | | | | | | | |
| FRU | Non-volatile | 1 | U4 | 2Kbit | EEPROM | No | Card manufacturing information | During Manufacturing, by programming the image via firmware update process. During runtime, by I2C Proprietary Command Protocol | no write protected | User cannot clear the memory. |
| MCU | Non-Volatile | 1 | U41 | 8kB | Flash ROM | No | BOSS-N1 information | The data is flash via iDRAC auto update | No write protected | User cannot clear the memory. |
| SPI flash | Non-Volatile | 1 | U5 | 128 Mb | SPI Flash EEPROM | Yes | Firmware, Boot code | Firmware and some configuration data flashed via Dell Update Package (DUP); some | no write protected | User cannot clear the memory. |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|--------------------|--------------------------|----------|----------------------|------------------|--------------------------------|---|--|--|---|---|
| | | | | | | | | configuration data is programmed during manufacturing; end user configuration data is written via UEFI HII | | |
| IDSDM | | | | | | | | | | |
| iDSDM (uSD1, uSD2) | Non-Volatile | 2 | J1, J2 | 16GB, 32GB, 64GB | NAND Flash | Yes | Provides mass storage | device resides in host domain; they are exposed to the user via an internally connected, non-removable USB mass storage device | physical write protect switch on ACE card | (1) card may be physically removed and destroyed or cleared via standard means on a separate computer OR (2) User has access to the card in the host domain and may clear it manually |
| SPI Flash | Non-Volatile | 1 | U2 | 8Mb | SPI Flash | SPI flash is only indirectly connected to iDRAC. | Boot firmware storage, configuration and state data for IDSDM. | User can initiate a firmware update of the IDSDM device. | There is no mechanism provided to iDRAC to write any SPI NOR area outside | iDRAC may issue a clear command to erase all contents of the SPI NOR, but doing this will leave |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|------------------|--------------------------|----------|----------------------|-------------------|--------------------------------|---|--|--|--|----------------------------|
| | | | | | | iDRAC can read any address in the SPI flash, but may only write the primary firmware storage area as a part of a firmware update procedure. | | | of the primary IDSDM firmware region. | the IDSDM non-functional. |
| LCD Bezel | | | | | | | | | | |
| MCU | Non-Volatile | 1 | IC1 | 2MB Flash in chip | Internal Flash | No | bootloader and s/w implementation of LCD command set | Updated as part of secure iDRAC software update. Configuration parameters can change only as part of | Writes are only allowed as part of secure iDRAC update | not user clearable. |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|------------|--------------------------|----------|----------------------|------|--------------------------------|---|---------------------------|---|---|-------------------------------|
| | | | | | | | | iDRAC update | | |
| R1T | | | | | | | | | | |
| MCU | Non-Volatile | 1 | U1 | 8kB | Flash ROM | No | Riser information | The data is flash via iDRAC auto update | No write protected. Not visible to Host Processor | User cannot clear the memory. |
| R1U | | | | | | | | | | |
| MCU | Non-Volatile | 1 | U1 | 8kB | Flash ROM | No | Riser information | The data is flash via iDRAC auto update | No write protected. Not visible to Host Processor | User cannot clear the memory. |
| R2A | | | | | | | | | | |
| MCU | Non-volatile | 1 | U1 | 8kB | Flash ROM | No | Riser information | The data is flash via iDRAC auto update | No write protected. Not visible to Host Processor | User cannot clear the memory. |
| R2T | | | | | | | | | | |
| MCU | Non-volatile | 1 | U1 | 8kB | Flash ROM | No | Riser information | The data is flash via iDRAC auto update | No write protected. Not visible to Host Processor | User cannot clear the memory. |
| R3A | | | | | | | | | | |
| MCU | Non- | 1 | U1 | 8kB | Flash ROM | No | Riser | The data is | No write | User cannot clear |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|------------|--------------------------|----------|----------------------|------|--------------------------------|---|---------------------------|---|---|-------------------------------|
| | volatile | | | | | | information | flash via iDRAC auto update | protected. Not visible to Host Processor | the memory. |
| R3B | | | | | | | | | | |
| MCU | Non-volatile | 1 | U1 | 8kB | Flash ROM | No | Riser information | The data is flash via iDRAC auto update | No write protected. Not visible to Host Processor | User cannot clear the memory. |
| R4A | | | | | | | | | | |
| MCU | Non-volatile | 1 | U1 | 8kB | Flash ROM | No | Riser information | The data is flash via iDRAC auto update | No write protected. Not visible to Host Processor | User cannot clear the memory. |
| R4P | | | | | | | | | | |
| MCU | Non-volatile | 1 | U1 | 8kB | Flash ROM | No | Riser information | The data is flash via iDRAC auto update | No write protected. Not visible to Host Processor | User cannot clear the memory. |
| R4Q | | | | | | | | | | |
| MCU | Non-volatile | 1 | U1 | 8kB | Flash ROM | No | Riser information | The data is flash via iDRAC auto update | No write protected. Not visible to Host Processor | User cannot clear the memory. |
| R4S | | | | | | | | | | |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|------|--------------------------|----------|----------------------|------|--------------------------------|---|---------------------------|---|---|-------------------------------|
| MCU | Non-volatile | 1 | U1 | 8kB | Flash ROM | No | Riser information | The data is flash via iDRAC auto update | No write protected. Not visible to Host Processor | User cannot clear the memory. |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|-------------|--------------------------|----------|----------------------|------|--------------------------------|---|---------------------------|-----------------------------------|-------------------------------------|--|
| PSU2800W | | | | | | | | | | |
| DELTA PSU | | | | | | | | | | |
| Primary MCU | Non-volatile | 1 | IC703 | 64KB | Internal Flash | No | Boot code, FW | The data is flash via Dell | SW write protected | Before firmware update, the memory will be |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|-------------------|--------------------------|----------|----------------------|------|--------------------------------|---|---------------------------|---|-------------------------------------|---|
| | | | | | | | | Update Package(DUP) | | cleared. |
| Secondary MCU | Non-volatile | 1 | IC805 | 64KB | Internal Flash | No | Boot code, FW | The data is flash via Dell Update Package(DUP) | SW write protected | Before firmware update, the memory will be cleared. |
| FRU | Non-volatile | 1 | IC704 | 16KB | EEPROM | No | PSU information | During Manufacturing , by programming the image via firmware update process | SW write protected | User cannot clear the memory. |
| LiteOn PSU | | | | | | | | | | |
| Primary MCU | Non-volatile | 1 | IC050 | 64K | Internal Flash | No | Boot code, FW | The data is flash via Dell Update Package(DUP) | SW write protected | Before firmware update, the memory will be cleared. |
| Secondary MCU/FRU | Non-volatile | 1 | IC900 | 128K | Internal Flash | No | Boot code, FW | The data is flash via Dell Update Package (DUP) | SW write protected | Before firmware update, the memory will be cleared. |
| PSU 2400W | | | | | | | | | | |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|-------------------|--------------------------|----------|----------------------|------|--------------------------------|---|---------------------------|---|-------------------------------------|---|
| DELTA PSU | | | | | | | | | | |
| Primary MCU | Non-volatile | 1 | IC703 | 64KB | Internal Flash | No | Boot code, FW | The data is flash via Dell Update Package (DUP) | SW write protected | Before firmware update, the memory will be cleared. |
| Secondary MCU | Non-volatile | 1 | IC805 | 64KB | Internal Flash | No | Boot code, FW | The data is flash via Dell Update Package (DUP) | SW write protected | Before firmware update, the memory will be cleared. |
| FRU | Non-volatile | 1 | IC704 | 16KB | EEPROM | No | PSU information | During Manufacturing , by programming the image via firmware update process | SW write protected | User cannot clear the memory. |
| LiteOn PSU | | | | | | | | | | |
| Primary MCU | Non-volatile | 1 | IC050 | 64K | Internal Flash | No | Boot code, FW | The data is flash via Dell Update Package (DUP) | SW write protected | Before firmware update, the memory will be cleared. |
| Secondary MCU/FRU | Non-volatile | 1 | IC900 | 128K | Internal Flash | No | Boot code, FW | The data is flash via Dell Update | SW write protected | Before firmware update, the memory will be cleared. |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|------|--------------------------|----------|----------------------|------|--------------------------------|---|---------------------------|-----------------------------------|-------------------------------------|----------------------------|
| | | | | | | | | Package (DUP) | | |



NOTE: For any information that you may need, direct your questions to your Dell Marketing contact.

02 - 2023

© 2023 Dell Inc. or its subsidiaries. All rights reserved. Dell and other trademarks are trademarks of Dell Inc. or its subsidiaries. Other trademarks may be trademarks of their respective owners.