DELL Technologies

Statement of Volatility – Dell PowerEdge R6625

Dell PowerEdge R6625 contains both volatile and non-volatile (NV) components. Volatile components lose their data immediately upon removal of power from the component. Non-volatile components continue to retain their data even after the power has been removed from the component. Components chosen as user-definable configuration options (those not soldered to the motherboard) are not included in the Statement of Volatility. Configuration option information (pertinent to options such as microprocessors, remote access controllers, and storage controllers) is available by component separately. The following NV components are present in the PowerEdge R6625 server.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
Planar										
CPU Internal CMOS RAM	Non-Volatile	1	U_CPU1	256 Bytes	Battery-backed CMOS RAM	No	Real-time clock and BIOS configuration settings	BIOS	N/A – BIOS only control	1) Set NVRAM_CLR jumper to clear BIOS configuration settings at boot and reboot system. 2) Power off the system, remove coin cell battery for 30 seconds, replace battery and then power back on. 3) Restore default configuration in F2 system setup menu.
BIOS SPI Flash	Non-Volatile	1	U174	32 MB	SPI Flash	No	Boot code, system configuration information,	SPI interface via CPU	Software write protected	Not possible with any utilities or applications and system is not functional if corrupted or removed.

							UEFI environment			
BIOS Data SPI Flash	Non-Volatile	1	U19	4 MB	SPI Flash	No	4MB Data SPI ROM storage BIOS setting.	SPI interface via CPU	Software write protected	Not possible with any utilities or applications and the system is not functional if BIOS SPI is corrupted or removed.
iDRAC SPI Flash	Non-Volatile	1	U29	4 MB	SPI Flash	No	iDRAC Uboot (boot loader), server management persistent store (i.e. iDRAC boot variables), and virtual planar FRU	SPI interface via iDRAC	Embedded iDRAC subsystem firmware actively controls sub area based write protection as needed.	The user cannot clear memory completely. However, user data, lifecycle log and archive, SEL, and firmware image repository can be cleared using Delete Configuration and Retire System, which can be accessed through the Lifecycle Controller interface.
BMC EMMC	Non-Volatile	1	U175	8 GB	eMMC NAND Flash	No	Operational iDRAC FW, Lifecycle Controller (LC) USC partition, LC service diags, LC OS drivers, USC firmware, IDRAC MAC Address, and EPPID, rac log, System Event Log, lifecycle log cache	NAND Flash interface via iDRAC	Embedded FW write protected	The user cannot clear memory completely. However, user data, lifecycle log and archive, SEL, and firmware image repository can be cleared using Delete Configuration and Retire System, which can be accessed through the Lifecycle Controller interface.

iDRAC DDR4	Volatile	1	U_IDRAC9_ DRAM1	8Gb	RAM	Yes	iDRAC RAM	iDRAC firmware	Not write-protected	Remove AC
System CPLD RAM	Volatile	1	U_CPLD1	432 kb	RAM	No	Not utilized	Not utilized	Not accessible	Not accessible
System CPLD Flash	Non-Volatile	1	U_CPLD1	448 kb	FLASH	No	Power on System Firmware	Firmware update	BIOS Security Protocols	Not user clearable
System Memory: RDIMM	Volatile	Up to 12	CPU1: A1 ~ A16	Up to 256GB per DIMM	RAM	Yes	System OS RAM	System OS	OS Control	Reboot or power down system
System Memory: RDIMM	Volatile	Up to 12	CPU2: B1 ~ B12	Up to 256GB per DIMM	RAM	Yes	System OS RAM	System OS	OS Control	Reboot or power down system
CPU _VDDCR_ CORE0, VDDCR_S OC, VDDIO , VDDCR_C ORE1 , and VDD11 Regulators	Non-Volatile	6	CPU1: U50, U123,U128, CPU2: U149, U158, U141	64KB	OTP (one time programmabl e)	No	Operational parameters	Once values are loaded into register space a cmd writes to nvm.	There are passwords for different sections of the register space	The user cannot clear memory.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
4 x3.5" SAS4/SATA BP										
SEP internal flash	Non-Volatile	1	U_46	4Mbit in-chip SPI Serial Flash	Integrated Flash+EEPROM	No	Firmware + FRU	I2C interface via iDRAC	Program write protect bit	Not user clearable
Backplane External FRU	Non-Volatile	1	U_46	256 Bytes	I2C EEPROM	No	FRU	Programmed at ICT during production.	No write protect	User cannot clear the memory.
8X2.5” Low Z Universal (SAS4/Gen4) BP										
SEP internal flash	Non-Volatile	1	U14	Flash: 512KB Data SRAM : 256KB Battery Powered Storage SRAM : 64B	Integrated Flash + Data SRAM + Battery Powered Storage SRAM	No	Firmware + FRU	I2C interface via iDRAC	Program write protect bit	Not user clearable
10X2.5” Universal (SAS4/Gen4) BP										

SEP internal flash	Non-Volatile	1	U14	Flash: 512KB Data SRAM : 256KB Battery Powered Storage SRAM : 64B	Integrated Flash + Data SRAM + Battery Powered Storage SRAM	No	Firmware + FRU	I2C interface via iDRAC	Program write protect bit	Not user clearable
8x EDSFF Passive BP										
SEP internal flash	Non-Volatile	1	U5	Flash: 512KB Data SRAM : 256KB Battery Powered Storage SRAM : 64B	Integrated Flash + Data SRAM + Battery Powered Storage SRAM	No	Firmware + FRU	I2C interface via iDRAC	Program write protect bit	Not user clearable
Rear X2 EDSFF BP										

SEP internal flash	Non-Volatile	1	U3	Flash: 512KB Data SRAM : 256KB Battery Powered Storage SRAM : 64B	Integrated Flash + Data SRAM + Battery Powered Storage SRAM	No	Firmware + FRU	I2C interface via iDRAC	Program write protect bit	Not user clearable
Rear 2x2.5 Universal Passive (SAS4) BP										
SEP internal flash	Non-Volatile	1	U47	Flash: 512KB Data SRAM : 256KB Battery Powered Storage SRAM : 64B	Integrated Flash + Data SRAM + Battery Powered Storage SRAM	No	Firmware + FRU	I2C interface via iDRAC	Program write protect bit	Not user clearable
HBA355i fPERC (Internal controller)										
SPI Flash	Non-Volatile	1	U2	128Mb	Flash	No	Card firmware	ROC writes configuration data	no write protected. Not visible to Host Processor	User cannot clear the memory.
FRU	Non-volatile	1	U5	2Kb	EEPROM	No	Card manufacture information	Programmed at ICT during production.	no write protected	User cannot clear the memory.

CPLD	Non-volatile	1	U23	24kb	Integrated Flash+EEPROM	No	Power sequencing and Cache Offload	Pre-programmed before assembly. Can be updated using Dell/LSI tools	no write protected. Not visible to Host Processor	User cannot clear the memory.
MCU	Non-volatile	1	U41	8KB	Integrated Flash+EEPROM	No	PCIe Bifurcation information to system iDRAC	Pre-programmed before assembly. Can be updated using Dell/LSI tools	no write protected. Not visible to Host Processor	User cannot clear the memory.
HBA355F fPERC (Internal controller)										
SPI Flash	Non-Volatile	1	U2	128Mb	EEPROM	No	Card firmware	ROC writes configuration data to NVSRAM	no write protected. Not visible to Host Processor	User cannot clear the memory.
FRU	Non-volatile	1	U5	2Kb	EEPROM	No	Card manufacture information	Programmed at ICT during production.	no write protected	User cannot clear the memory.
CPLD	Non-volatile	1	U23	24kb	Integrated Flash+EEPROM	No	Power sequencing and Cache Offload	Pre-programmed before assembly. Can be updated using Dell/LSI tools	no write protected. Not visible to Host Processor	User cannot clear the memory.
MCU	Non-volatile	1	U41	8KB	Integrated Flash+EEPROM	No	PCIe Bifurcation information to system iDRAC	Pre-programmed before assembly. Can be updated using Dell/LSI tools	no write protected. Not visible to Host Processor	User cannot clear the memory.
H755 PERC (Internal Controller)										
SDRAM	Volatile	9	U1077~U1085	8GB	SDRAM	No	Cache for HDD I/O	ROC writes to this memory - using it as cache for data IO to HDDs	no write protected. Not visible to Host Processor	Cache can be cleared by powering off the card
ONFI	Non-volatile	1	U1100	512Gb	NAND Flash	No	Memory for backup storage for DDR4	ROC backs up DDR data to this device in case of a power failure	no write protected. Not visible to Host Processor	User cannot clear the memory.

BMU	Non-Volatile	1	U1126	180KB	Integrated Flash+EEPROM	No	Battery Management control	Programmed at ICT during production	no write protected. Not visible to Host Processor	User cannot clear the memory.
SPI Flash	Non-Volatile	1	U1086	128Mb	SPI Flash	No	Firmware	Pre-programmed before assembly. Can be updated using Dell/LSI tools	no write protected. Not visible to Host Processor	User can clear the memory.
NVSRAM	Non-volatile	1	U1087	128KB	NVSRAM	No	Configuration data	ROC writes configuration data to NVSRAM	no write protected. Not visible to Host Processor	
FRU	Non-volatile	1	U1019	2Kb	EEPROM	No	Card manufacturing information	Programmed at ICT during production.	no write protected	User cannot clear the memory.
SPD	Non-volatile	1	U22	2Kb	EEPROM	No	Memory configuration data	Programmed at ICT during production. ROC read the configured data from the SPD for DDR settings	no write protected. Not visible to Host Processor	User cannot clear the memory.
CPLD	Non-volatile	1	U1088	64kb	Integrated Flash+EEPROM	No	Power sequencing and Cache Offload	Pre-programmed before assembly. Can be updated using Dell/LSI tools	no write protected. Not visible to Host Processor	User cannot clear the memory.
MCU	Non-volatile	1	U41	8KB	Integrated Flash+EEPROM	No	PCIe Bifurcation information to system iDRAC	Pre-programmed before assembly. Can be updated using Dell/LSI tools	no write protected. Not visible to Host Processor	User cannot clear the memory.
H755N PERC (Internal Controller)										
SDRAM	Volatile	9	U1077~U1085	8GB	SDRAM	No	Cache for HDD I/O	ROC writes to this memory - using it as cache for data IO to HDDs	no write protected. Not visible to Host Processor	Cache can be cleared by powering off the card

ONFI	Non-volatile	1	U1100	512Gb	NAND Flash	No	Memory for backup storage for DDR4	ROC backs up DDR data to this device in case of a power failure	no write protected. Not visible to Host Processor	User cannot clear the memory.
BMU	Non-Volatile	1	U1126	180KB	Integrated Flash+EEPROM	No	Battery Management control	Programmed at ICT during production	no write protected. Not visible to Host Processor	User cannot clear the memory.
SPI Flash	Non-Volatile	1	U1086	128Mb	SPI Flash	No	Firmware	Pre-programmed before assembly. Can be updated using Dell/LSI tools	no write protected. Not visible to Host Processor	User can clear the memory.
NVSRAM	Non-volatile	1	U1087	128KB	NVSRAM	No	Configuration data	ROC writes configuration data to NVSRAM	no write protected. Not visible to Host Processor	
FRU	Non-volatile	1	U1019	2Kb	EEPROM	No	Card manufacturing information	Programmed at ICT during production.	no write protected	User cannot clear the memory.
SPD	Non-volatile	1	U22	2Kb	EEPROM	No	Memory configuration data	Programmed at ICT during production. ROC read the configured data from the SPD for DDR settings	no write protected. Not visible to Host Processor	User cannot clear the memory.
CPLD	Non-volatile	1	U1088	64kb	Integrated Flash+EEPROM	No	Power sequencing and Cache Offload	Pre-programmed before assembly. Can be updated using Dell/LSI tools	no write protected. Not visible to Host Processor	User cannot clear the memory.
MCU (Cordova)	Non-volatile	1	U41	8KB	Integrated Flash+EEPROM	No	PCIe Bifurcation information to system iDRAC	Pre-programmed before assembly. Can be updated using Dell/LSI tools	no write protected. Not visible to Host Processor	User cannot clear the memory.
H965i PERC (Internal Controller)										

SDRAM	Volatile	9	U1077~U1085	8GB	SDRAM	No	Cache for HDD I/O	ROC writes to this memory - using it as cache for data IO to HDDs	no write protected. Not visible to Host Processor	Cache can be cleared by powering off the card
ONFI	Non-volatile	1	U1100	512Gb	ONFI Nand	No	Memory backup storage for DDR4	ROC backs up DDR data to this device in case of a power failure	no write protected. Not visible to Host Processor	User cannot clear the memory.
BMU	Non-Volatile	1	U1126	180KB	Integrated Flash+EEPROM	No	Memory configuration data	Pre-programmed before assembly. Can be updated using Dell/LSI tools	no write protected. Not visible to Host Processor	User cannot clear the memory.
SPI Flash	Non-Volatile	1	U2	128Mb	SPI Flash	No	Firmware	Pre-programmed before assembly. Can be updated using Dell/LSI tools	no write protected. Not visible to Host Processor	User can clear the memory.
NVSRAM	Non-volatile	1	U1087	128KB	SDRAM	No	Power sequencing and Cache Offload	ROC writes configuration data to NVSRAM	no write protected. Not visible to Host Processor	User cannot clear the memory.
FRU	Non-volatile	1	U1019	2Kb	EEPROM	No	Holds cache data during power loss	Programmed at ICT during production.	no write protected	User cannot clear the memory.
SPD	Non-volatile	1	U22	2Kb	EEPROM	No	Cache for HDD I/O	Pre-programmed before assembly	no write protected. Not visible to Host Processor	User cannot clear the memory.
CPLD	Non-volatile	1	U1088	64kb	Integrated Flash+EEPROM	No	Power sequencing and Cache Offload	Pre-programmed before assembly. Can be updated using Dell/LSI tools	no write protected. Not visible to Host Processor	User cannot clear the memory.

Item	**Non-Volatile or**	**Quantity**	**Reference Designator**	**Size**	**Type (e.g. Flash PROM, EEPROM)**	**Can user programs or operating**	**Purpose? (e.g. boot code)**	**How is data input to this memory?**	**How is this memory write protected?**	**How is the memory cleared?**

	Volatile					**system write data to it during normal operation?**				
Status LED Control Panel										
Microcontroller	Non-Volatile	1	U_TINY	8KB	Flash	No	Driving Health and Status LED	I2C via iDRAC	Hardware strapping	User cannot clear the memory.
Standard/LC RIO										
MCU	Non-Volatile	1	U6	8kB	Flash ROM	No	Standard /LC RIO information	The data is flash via iDRAC auto update	No write protected. Not visible to Host Processor	User cannot clear the memory.
Power Button Control Panel										
SPI Flash	Non-Volatile	1	U2	32 Mb	SPI Flash	No	Easy Restore functionality contains Service Tag, Copy of SEL logs	SPI interface from iDRAC to Right Cntl Panel	Embedded iDRAC subsystem firmware actively controls sub area based write protection as needed.	The user cannot clear memory.
LOM										
SPI Flash	Non-Volatile	1	U1	8-Mbit DataFlash (with Extra 256-Kbits)	SPI Flash EEPROM	Yes	Firmware, configuration data	Firmware and some configuration data flashed via Dell Update Package (DUP); some configuration data is programmed during	Reserving write protection function for HW design.	User cannot clear the memory.

								manufacturing; end user configuration data is written via UEFI HII		
MCU	Non-Volatile	1	U2	64KB Flash and 8KB of SRAM	Flash ROM	No	LOM Security data	Off-line programming Before production	No write protected. Not visible to Host Processor	User cannot clear the memory
Left Titan2										
MCU	Non-Volatile	1	USAM7	2MB Flash in chip	SPI FlashN	No	For field maintenance. Have License, Service Tag and system information. Driving health and status LEDs	SPI interface via iDRAC	Hardware strapping	User cannot clear the memory.
TPM										
Trusted Platform Module (TPM)	Non-Volatile	1	U2	128 Bytes	EEPROM	Yes	Storage of encryption keys	Using TPM Enabled operating systems	SW write protected	F2 Setup option
BOSS N1										
FRU	Non-volatile	1	U4	2Kbit	EEPROM	No	Card manufacturing information	During Manufacturing, by programming the image via firmware update process.	no write protected	User cannot clear the memory.

								During runtime, by I2C Proprietary Command Protocol		
MCU	Non-Volatile	1	U41	8kB	Flash ROM	No	BOSS-N1 information	The data is flash via iDRAC auto update	No write protected	User cannot clear the memory.
SPI flash	Non-Volatile	1	U5	128 Mb	SPI Flash EEPROM	Yes	Firmware, Boot code	Firmware and some configuration data flashed via Dell Update Package (DUP); some configuration data is programmed during manufacturing; end user configuration data is written via UEFI HII	no write protected	User cannot clear the memory.
IDSDM										
iDSDM (uSD1, uSD2)	Non-Volatile	2	J1, J2	16GB, 32GB, 64GB	NAND Flash	Yes	Provides mass storage	device resides in host domain; they are exposed to the user via an internally connected, non-removable USB mass storage device	physical write protect switch on ACE card	(1) card may be physically removed and destroyed or cleared via standard means on a separate computer OR (2)User has access to the card in the host domain and may clear it manually

SPI Flash	Non-Volatile	1	U2	8Mb	SPI Flash	SPI flash is only indirectly connected to iDRAC. iDRAC can read any address in the SPI flash, but may only write the primary firmware storage area as a part of a firmware update procedure.	Boot firmware storage, configuration and state data for IDSDM.	User can initiate a firmware update of the IDSDM device.	There is no mechanism provided to iDRAC to write any SPI NOR area outside of the primary IDSDM firmware region.	iDRAC may issue a clear command to erase all contents of the SPI NOR, but doing this will leave the IDSDM non-functional.
LCD Bezel										
MCU	Non-Volatile	1	IC1	2MB Flash in chip	Internal Flash	No	bootloader and s/w implementation of LCD command set	Updated as part of secure iDRAC software update. Configuration parameters can change only as part of iDRAC update	Writes are only allowed as part of secure iDRAC update	not user clearable.
R1P										

MCU	Non-Volatile	1	U1	8kB	Flash ROM	No	Riser information	The data is flash via iDRAC auto update	No write protected. Not visible to Host Processor	User cannot clear the memory.
R2A										
MCU	Non-Volatile	1	U1	8kB	Flash ROM	No	Riser information	The data is flash via iDRAC auto update	No write protected. Not visible to Host Processor	User cannot clear the memory.
R2Q										
MCU	Non-Volatile	1	U1	8kB	Flash ROM	No	Riser information	The data is flash via iDRAC auto update	No write protected. Not visible to Host Processor	User cannot clear the memory.
R2S										
MCU	Non-Volatile	1	U1	8kB	Flash ROM	No	Riser information	The data is flash via iDRAC auto update	No write protected. Not visible to Host Processor	User cannot clear the memory.
R3A										
MCU	Non-Volatile	1	U1	8kB	Flash ROM	No	Riser information	The data is flash via iDRAC auto update	No write protected. Not visible to Host Processor	User cannot clear the memory.
R3P										
MCU	Non-Volatile	1	U1	8kB	Flash ROM	No	Riser information	The data is flash via iDRAC auto update	No write protected. Not visible to Host Processor	User cannot clear the memory.
R3S										
MCU	Non-Volatile	1	U1	8kB	Flash ROM	No	Riser information	The data is flash via iDRAC auto update	No write protected. Not	User cannot clear the memory.

									visible to Host Processor	
R4-E3 Gen5 Paddle card										
MCU	Non-Volatile	1	U1	8kB	Flash ROM	No	Riser information	The data is flash via iDRAC auto update	No write protected. Not visible to Host Processor	User cannot clear the memory.
R4-SCM G5x4 Paddle card										
MCU	Non-Volatile	1	U1	8kB	Flash ROM	No	Riser information	The data is flash via iDRAC auto update	No write protected. Not visible to Host Processor	User cannot clear the memory.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
PSU										
DELTA PSU (1100W, 1400W, 1800W)										
Primary MCU	Non-volatile	1	IC703	64KB	Internal Flash	No	Boot code, FW	The data is flash via Dell Update Package (DUP)	SW write protected	Before firmware update, the memory will be cleared.
Secondary MCU	Non-volatile	1	IC805	64KB	Internal Flash	No	Boot code, FW	The data is flash via Dell Update Package (DUP)	SW write protected	Before firmware update, the memory will be cleared.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
FRU	Non-volatile	1	IC704	16KB	EEPROM	No	PSU information	During Manufacturing, by programming the image via firmware update process	SW write protected	User cannot clear the memory.
LiteOn PSU (800W, 1100W, 1400W, 1800W)										
Primary MCU	Non-volatile	1	IC050	64K	Internal Flash	No	Boot code, FW	The data is flash via Dell Update Package (DUP)	SW write protected	Before firmware update, the memory will be cleared.
Secondary MCU/FRU	Non-volatile	1	IC900	128K	Internal Flash	No	Boot code, FW	The data is flash via Dell Update Package (DUP)	SW write protected	Before firmware update, the memory will be cleared.
AEI PSU (800W, 1100W, 1400W)										
Primary MCU	Non-volatile	1	U317 (TI)	64K	Internal Flash	No	Boot code, FW	The data is flash via Dell Update Package (DUP)	SW write protected	Before firmware update, the memory will be cleared.
Secondary MCU	Non-volatile	2	U301 (TI) U315 (ST)	32K 128K	Internal Flash	No	Boot code, FW	The data is flash via Dell	SW write protected	Before firmware update, the memory will be cleared.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
								Update Package (DUP)		
FRU	Non-volatile	1	U305	2Mb	SERIAL FLASH	No	PSU information	During Manufacturing	SW write protected	User cannot clear the memory.

NOTE: For any information that you may need, direct your questions to your Dell Marketing contact.

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