

Technical Datasheet

ET6402-10AOC-7M-C

Edgecore® Compatible 40Gb/s QSFP+ to 4SFP+ Active Optical Breakout Cable, 7m

FEATURES

- Available lengths 7m to 100m
- Compliant with SFF-8436 for QSFP+ and standard SFF-8431 for SFP+
- High speed, high density. Supports up to 4X10Gb/s bi-directional operation
- Reliable VCSEL and PIN photonic devices
- I2C standard management interface
- Excellent high speed signal integrity
- Operating temperature: 0 to 70°C
- RoHS6 Compliant

APPLICATIONS

10G/40G Ethernet
Proprietary high speed, high density data
High performance computing, server and data storage

DESCRIPTION

ATGBICS ET6402-10AOC-7M-C is a 40Gb/s QSFP+ to 4x 10G SFP+ hot pluggable Active Optical Cable for Infiniband and Ethernet data transmission. It provides parallel interconnects: 4 transmitting / 4 receiving data lanes and supports distance up to 100 meters.

It is composed of optical transceivers on both ends with multimode fiber cable in between. This integrated optical module solution removes the complicated optical fiber interface and brings friendly and intuitive electrical-to-electrical interface to users.

This product is designed to meet the requirements of high speed, high density and low power consumption for applications in today's data centers.

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Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit
Storage Temperature	T _s	-40		+85	°C
Case Operating Temperature	T _A	0		70	°C
Maximum Supply Voltage	V _{cc}	0		3.6	V
Relative Humidity	RH	5		85	%

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	TC	0	25	70	°C
Supply Voltage	V _{cc}	3.135	3.3	3.465	V
Data Rate	-	-	4*10.3	-	Gb/s

Transceiver Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Low speed output: Transmitter Fault(TX_FAULT) /Loss of Signal (LOS)	VOH	2.0	-	V _{cc}	V	1
	VOL	0		0.8	V	1
Low speed input: Transmitter Disable (TX_DISABLE), MOD_DEF 1, MOD_DEF 2	VIH	2.0		V _{cc}	V	2
	VIL	-	-	0.8	V	2
Clock Rate-I2C	f	-	-	400	kHz	3
Module Turn-on time	-	-	-	2000	ms	4

Notes:

1. For all control input pins: LPMode, Reset and ModSelL.
2. For all status output pins: ModPrsL, IntL.
3. For management interface.
4. Time from module power-on / insertion/ ResetL deassert to module full functional.

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Transmitter Optical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit
Reference Differential Input Impedance	Zd	-	100	-	Ω
Optical Return Loss Tolerance	-	-	12	-	dB
Differential Data Input Swing	Vin_pp	180	-	700	mV
Differential Data Input Threshold	-	-	50	-	mV

Notes:

1. AC coupled inside AOC module.
2. Input swing to trigger TX-squelch.

Receiver Optical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Reference Differential Input Impedance	Zd	-	100	-	Ω	1
Pre-emphasis Pulse Amplitude Percentage	-	0	-	-	%	2
	-	10	-	-	%	
	-	20	-	-	%	
	-	40	-	-	%	
Pre-emphasis Pulse Duration	-	-	30	-	ps	
Signal Speed	-	-	10.3	-	Gb/s	-
Differential Data Input Swing	-	150	-	850	mV	-
Differential Data Output Swing When Squelched	-	-	-	50	mV	-
Rise / Fall Time (20% ~80%)	-	24			Ps	-

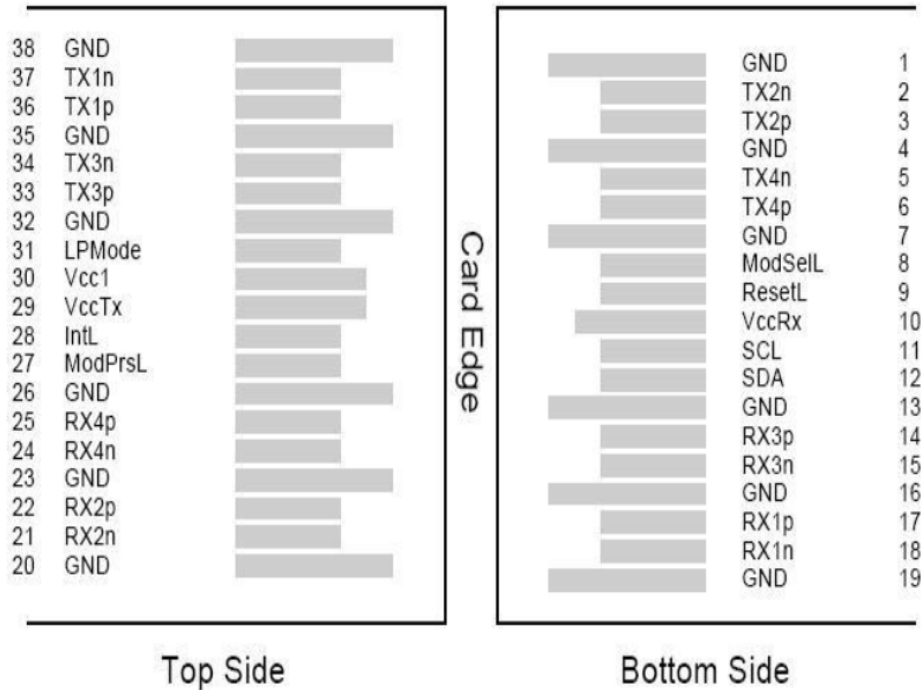
Notes:

1. AC coupled inside AOC module.
2. User selectable. Percentage is the ratio of pre-emphasis amplitude to output swing. Users could change by writing to page 3 address 237, default value is "10"

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Pin Assignment

Host PCB QSFP+ pad assignment top view



Pin Description for QSFP+

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Output	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Output	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVC MOS-I/O	SDA	2-Wire Serial Interface Data	

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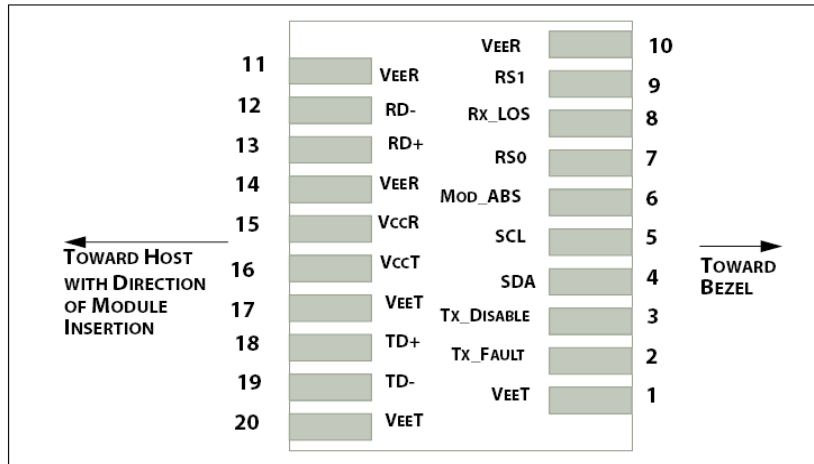
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Inverted Data Output	
15	CML-O	Rx3n	Receiver Non-Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Inverted Data Output	
18	CML-O	Rx1n	Receiver Non-Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply Transmitter	2
30		Vcc1	+3.3V Power Supply	2
31	LVTTL-I	LPMODE	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Inverted Data Output	
34	CML-I	Tx3n	Transmitter Non-Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Inverted Data Output	
37	CML-I	Tx1n	Transmitter Non-Inverted Data Output	
38		GND	Ground	1

Notes:

1. The module signal grounds are isolated from the module case.
2. This is an open collector/drain output that on the host board requires a 4.7KΩ to 10KΩ pull-up resistor to VccHost.

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Host PCB SFP+ pad assignment top view



Pin Description for SFP+

PIN #	Name	Function	Notes
1	VeeT	Module transmitter ground	1
2	Tx Fault	Module transmitter fault	2
3	Tx Disable	Transmitter Disable; Turns off transmitter laser output	3
4	SDL	2 wire serial interface data input/output (SDA)	
5	SCL	2 wire serial interface clock input (SCL)	
6	MOD-ABS	Module Absent, connect to VeeR or VeeT in the module	2
7	RS0	Rate select0, optionally control SFP+ receiver. When high, input data rate >4.5Gb/ s; when low, input data rate <=4.5Gb/s	
8	LOS	Receiver Loss of Signal Indication	4
9	RS1	Rate select0, optionally control SFP+ transmitter. When high, input data rate >4.5Gb/s; when low, input data rate <=4.5Gb/s	
10	VeeR	Module receiver ground	1
11	VeeR	Module receiver ground	1
12	RD-	Receiver inverted data out put	
13	RD+	Receiver non-inverted data out put	
14	VeeR	Module receiver ground	1
15	VccR	Module receiver 3.3V supply	
16	VccT	Module transmitter 3.3V supply	

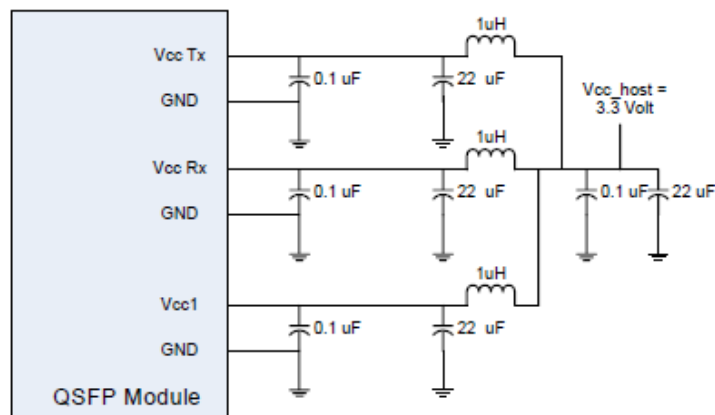
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17	VeeT	Module transmitter ground	1
18	TD+	Transmitter inverted data out put	
19	TD-	Transmitter non-inverted data out put	
20	VeeT	Module transmitter ground	1

Notes:

1. The module signal grounds are isolated from the module case.
2. This is an open collector/drain output that on the host board requires a 4.7KΩ to 10KΩ pull-up resistor to VccHost.
3. This input is internally biased high with a 4.7KΩ to 10KΩ pull-up resistor to VccT.
4. Two-Wire Serial interface clock and data lines require an external pull-up resistor dependent on the capacitance load.
5. This is a ground return that on the host board requires a 4.7KΩ to 10KΩ pull-up resistor to VccHost.

Recommended Application Interface Circuit



Recommended Host Board Power Supply Filter Network

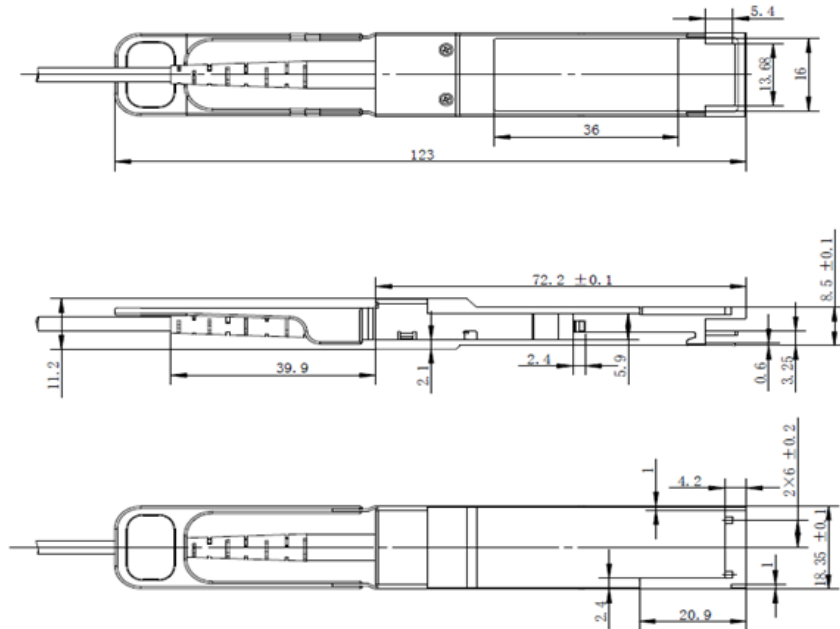
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Mechanical specifications

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
AOC cable length (L ≤ 7m)	L	L-0.06	L	L+0.06	M	-
AOC cable length (L > 7m)	L	L-(L*1.1%)	L	L+(L*1.1%)	M	-
Module Retention	-	90	-	170	N	-
Module Insertion	-	0	-	18	N	-
Module Extraction	-	0	-	25	N	-
Cable Pull Strength – Apply Load at 0°	-	44	-	-	N	-
Cable Pull Strength – Apply Load at 90°	-	33	-	-	N	-
Clearance Out of IO Bezel	-	75	-	-	nm	-
Cable Bending Radius	-	30	-	-	nm	-
Insertion / Removal Cycles	-	50	-	-	cycles	-

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Outline Drawing for QSFP



Outline Drawing for SFP+

