ATGBICS® by APPROVED TECHNOLOGY

Technical Datasheet

QSFP-100G-SR4-I

100GBase-SR4 QSFP28 Transceiver

Hot Pluggable, +3.3V, MPO, 850nm, up to 100m, Industrial Temperature

FEATURES

- Support 100GBASE-SR4/100G Fiber Channel application
- Compliant to QSFP28 Electrical MSA SFF-8636
- Multi rate of up to 25.78125Gbps
- Transmission distance up to 100m (OM4)
- +3.3V single power supply
- Low power consumption
- Industrial Operating case temperature: -40 to 85
- RoHS compliant

APPLICATIONS

- 100GBASE-SR4 at 25.78125Gbps per lane
- InfiniBand QDR, EDR
- Other optical links

DESCRIPTION

ATGBICS QSFP-100G-SR4-I transceiver is a Four-Channel, Pluggable, Parallel, Fibre-Optic QSFP28 transceiver for IEEE 802.3bm, 100GBASE-SR4 applications, or 40 Gigabit Ethernet and InfiniBand FDR/EDR applications. The QSFP28 full-duplex optical module offers 4 independent transmit and receive channels, each capable of 26Gbps operation for an aggregate data rate of 100Gbps 100m using OM4 fibre. These modules are designed to operate over multimode fibre systems using 850nm VCSEL laser array. An optical fibre ribbon cable with an MPO/MTP® connector can be plugged into the QSFP module receptacle. QSFP28 SR4 is one kind of parallel transceiver which provides increased port density and total system cost savings.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	85	℃
Supply Voltage	Vcc	-0.5	3.6	V
Operating Humidity	RH	5	85	%
Receiver Damage Threshold per Lane	PIND	3.4		dBm

RECOMMENDED OPERATING ENVIRONMENT

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	T_C	-40		85	℃
Power Supply Voltage	Vcc	3.14	3.3	3.47	V
Power Dissipation	Pd	-		2.5	W
Bit Rate	BR	10.3125	25.78125		Gbps

OPTICAL CHARACTERISTICS

Parameter	Symbol	Min	Typical	Max	Unit	Notes
TRANSMITTER						
Bit Rate	BR	10.3125	25.78125		Gbps	
Centre Wavelength Range	λC	840	850	860	nm	
RMS Spectral Width	Δλ			0.6	nm	
Average Launch Power Tx_off	Poff			-30	dBm	
Launch Optical Power	P0	-6.0		2.4	dBm	1
Extinction Ratio	ER	2			dB	
RECEIVER						
Bit Rate	BR	10.3125	25.78125		Gbps	
Sensitivity@ BER=E- 12	THd			-5.2	dBm	
Sensitivity@ BER=5E-5	OVL	+2.4			dBm	
Overload Input Optical Power	SEN			-10.3	dBm	2
Centre Wavelength Range	λC	840		860	nm	
LOS Assert		-30			dBm	
LOS De-Assert				-12	dBm	
LOS Hysteresis		0.5			dB	

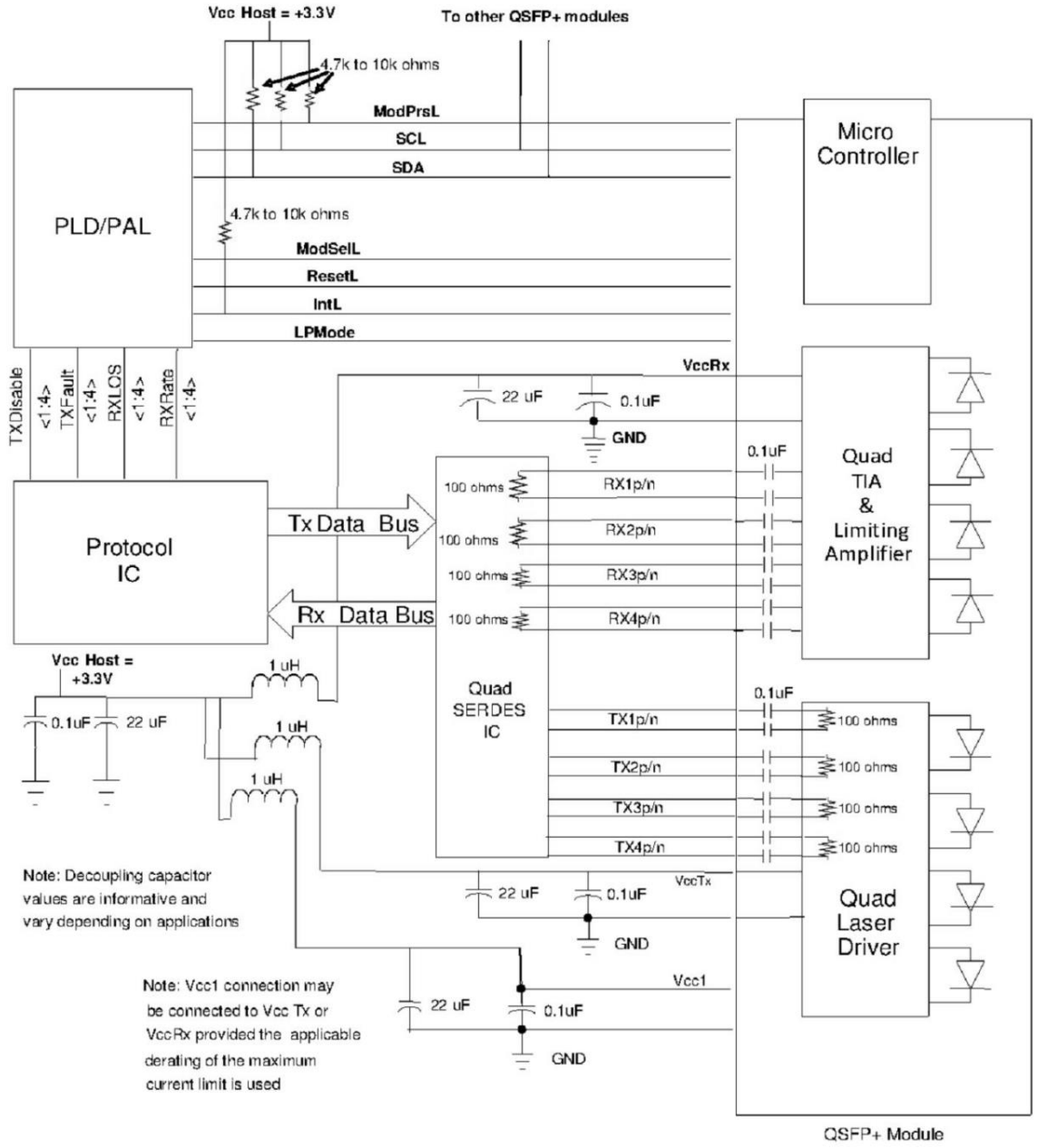
Notes:

1. Coupled into 50/135 MMF
2. Measured with PRBS 2^31 -1 test pattern @25.78125Gbps.BER=E-12

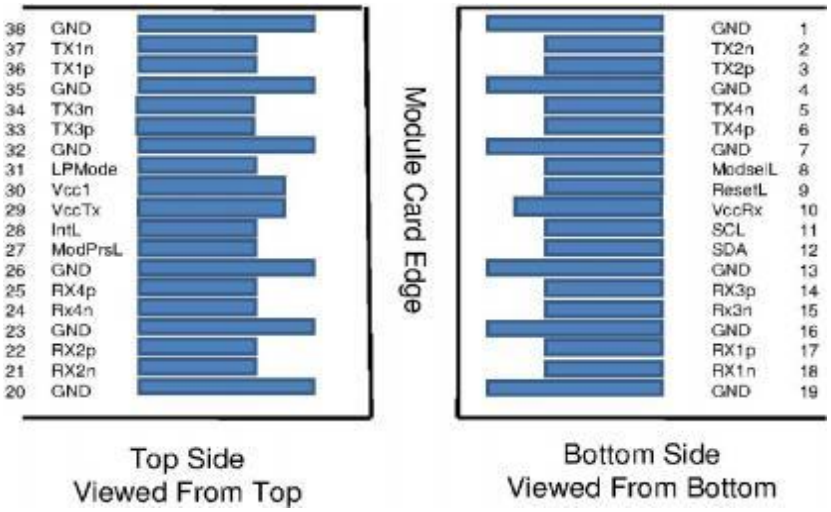
ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Input Logic Level High	VIH	2.0	-	VCC+0.3	V	
Input Logic Level Low	VIL	VEE-0.3	-	0.8	V	
Output Logic Level High	VOH	2.0	-	VCC+0.3	V	
Output Logic Level Low	VOL	0	-	0.4	V	
TRANSMITTER						
Differential Data Input Swing	Vin,P-P	200	-	1000	mVPP	
Input Differential Impedance	ZIN	90	100	110	Ω	
RECEIVER						
Differential Date Output Swing	Vout	200	-	1000	mV	
Output Differential Impedance	ZD	90	100	110	Ω	

RECOMMENDED INTERFACE CIRCUIT



PIN ARRANGEMENT



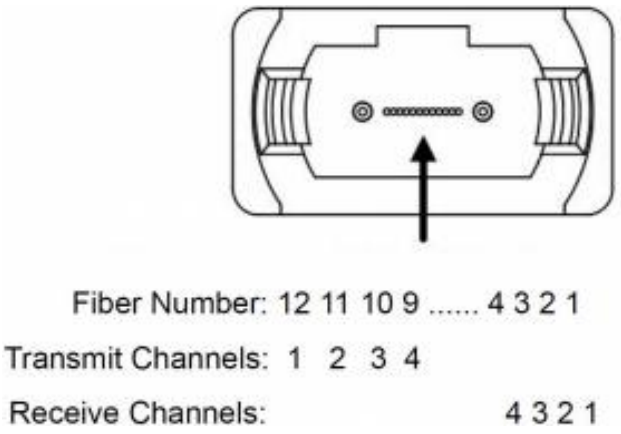
PIN FUNCTION DEFINITIONS

Pin	Symbol	Name/ Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non- Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non- Inverted Data Input	
7	GND	Ground	1
8	ModSel L	Modu le Select	
9	Reset L	Modu le Reset	
10	Vcc Rx	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Receiver Non- Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non- Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non- Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non- Inverted Data Output	
26	GND	Ground	1
27	Mod PrsL	Module Present	
28	Int L	Interrupt	
29	Vcc Tx	+3 .3V Power supply transmitter	
30	Vcc1	+3 .3V Power supply	
31	LPMode	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non- Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non- Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Note:

1. Circuit ground is internally isolated from chassis ground

OPTICAL INTERFACE ARRANGEMENT



Optical interface arrangement, Lens upwards

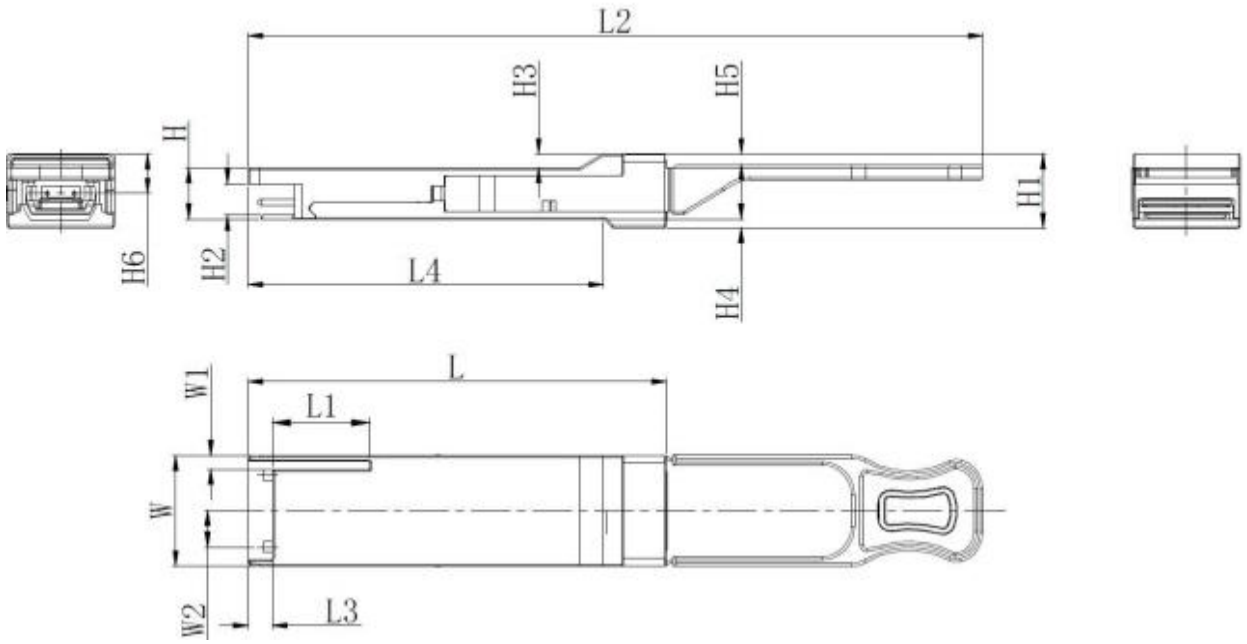
MONITORING SPECIFICATION

2-Wire Serial Address 1010000x
Lower Page 00h
0 Identifier
1- 2 Status
3- 21 Interrupt Flags
22- 33 Free Side Device Monitors
34- 81 Channel Monitors
82- 85 Reserved
86- 98 Control
99 Reserved
100-104 Hardware Interrupt Pin Masks
105-106 Vendor Specific
107 Reserved
108-110 Free Side Device Properties
111-112 Assigned for use by PCI Express
113 Free Side Device Properties
114-118 Reserved
119-122 Password Change Entry Area (Optional)
123-126 Password Entry Area (Optional)
127 Page Select Byte

Upper Page 00h	Optional Page 01h	Optional Page 02h	Optional Page 03h
128 Identifier	128 CC_APPS	128-255 User EEPROM Data	128-175 Free Side Device Thresholds
129-191 Base ID Fields	129 AST Table Length (TL)		
	130-131 Application Code Entry 0		
	132-133 Application Code Entry 1		
	134-253 other entries		176-223 Channel Thresholds
192-223 Extended ID			224 Tx EQ & Rx Emphasis Magnitude ID
224-255 Vendor Specific ID			225 RX output amplitude indicators
			226-241 Channel Controls
			242-251 Channel Monitor Masks
	254-255 Application Code Entry TL		252-255 Reserved

Memory Map

MECHANICAL DIMENSIONS



Unit: mm

	L	L1	L2	L3	L4	W	W1	W2	H	H1	H2	H3	H4	H5	H6
Max	72.2	-	128	4.35	61.4	18.45	-	6.2	8.6	12.4	5.35	2.5	1.6	2.0	-
Type	72.0	-	-	4.20	61.2	18.35	-	-	8.5	12.2	5.2	2.3	1.5	1.8	6.55
Min	68.8	16.5	124	4.05	61.0	18.25	2.2	5.8	8.4	12.0	5.05	2.1	1.3	1.6	-