DELL Technologies

# Statement of Volatility – Dell PowerEdge R660

Dell PowerEdge R660 contains both volatile and non-volatile (NV) components. Volatile components lose their data immediately upon removal of power from the component. Non-volatile components continue to retain their data even after the power has been removed from the component. Components chosen as user-definable configuration options (those not soldered to the motherboard) are not included in the Statement of Volatility. Configuration option information (pertinent to options such as microprocessors, remote access controllers, and storage controllers) is available by component separately. The following NV components are present in the PowerEdge R660 server.

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---|---|---|---|---|---|---|---|---|---|---|
| **Planar** | | | | | | | | | | |
| PCH Internal CMOS RAM | Non-Volatile | 1 | U_PCH1 | 256 Bytes | Battery-backed CMOS RAM | No | Real-time clock and BIOS configuration settings | BIOS | N/A – BIOS only control | 1) Set NVRAM_CLR jumper to clear BIOS configuration settings at boot and reboot system.<br>2) Power off the system, remove coin cell battery for 30 seconds, replace battery and then power back on.<br>3) Restore default configuration in F2 system setup menu. |
| BIOS SPI Flash | Non-Volatile | 1 | U121 | 32 MB | SPI Flash | No | Boot code, system configuration information, UEFI | SPI interface via PCH | Software write protected | Not possible with any utilities or applications and system is not functional if corrupted or removed. |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | environment, ME | | | |
| BIOS Data SPI Flash | Non-Volatile | 1 | U19 | 4 MB | SPI Flash | No | 4MB Data SPI ROM storage BIOS setting. | SPI interface via PCH | Software write protected | Not possible with any utilities or applications and the system is not functional if BIOS SPI is corrupted or removed. |
| iDRAC SPI Flash | Non-Volatile | 1 | U29 | 4 MB | SPI Flash | No | iDRAC Uboot (boot loader), server management persistent store (i.e. iDRAC boot variables), and virtual planar FRU | SPI interface via iDRAC | Embedded iDRAC subsystem firmware actively controls sub area based write protection as needed. | The user cannot clear memory completely. However, user data, lifecycle log and archive, SEL, and firmware image repository can be cleared using Delete Configuration and Retire System, which can be accessed through the Lifecycle Controller interface. |
| BMC EMMC | Non-Volatile | 1 | U122 | 8 GB | eMMC NAND Flash | No | Operational iDRAC FW, Lifecycle Controller (LC) USC partition, LC service diags, LC | NAND Flash interface via iDRAC | Embedded FW write protected | The user cannot clear memory completely. However, user data, lifecycle log and archive, SEL, and firmware image repository can be cleared |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | OS drivers, USC firmware, IDRAC MAC Address, and EPPID, rac log, System Event Log, lifecycle log cache | | | using Delete Configuration and Retire System, which can be accessed through the Lifecycle Controller interface. |
| iDRAC DDR4 | Volatile | 1 | U_IDRAC9_DRAM1 | 8Gb | RAM | Yes | iDRAC RAM | iDRAC firmware | Not write-protected | Remove AC |
| System CPLD RAM | Volatile | 1 | U_CPLD1 | 432 kb | RAM | No | Not utilized | Not utilized | Not accessible | Not accessible |
| System CPLD Flash | Non-Volatile | 1 | U_CPLD1 | 448 kb | FLASH | No | Power on System Firmware | Firmware update | BIOS Security Protocols | Not user clearable |
| System Memory: RDIMM | Volatile | Up to 32 | CPU1: A1~16 CPU2: B1~B16 | Up to 256GB per DIMM | RAM | Yes | System OS RAM | System OS | OS Control | Reboot or power down system |
| CPU VCCIN and FIVRA Regulators | Non-Volatile | 2 | U50, U69 | 64KB | OTP (one time programmable) | No | Operational parameters | Once values are loaded into register space a cmd writes to nvm. | There are passwords for different sections of the register space | The user cannot clear memory. |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---|---|---|---|---|---|---|---|---|---|---|
| CPU INFAON and VCCFA Regulators | Non-Volatile | 2 | U105, U106 | 64KB | OTP (one time programmable) | No | Operational parameters | Once values are loaded into register space a cmd writes to nvm. | There are passwords for different sections of the register space | The user cannot clear memory. |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---|---|---|---|---|---|---|---|---|---|---|
| **8x2.5" Universal Smart Flow Backplane** | | | | | | | | | | |
| SEP internal flash | Non-Volatile | 1 | U14 | Flash: 512KB<br><br>Data SRAM : 256KB | Integrated Flash + Data SRAM + Battery Powered Storage SRAM | No | Firmware + FRU | I2C interface via iDRAC | Program write protect bit | Not user clearable |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Battery Powered Storage SRAM : 64B | | | | | | |
| **10x2.5" Universal Backplane** | | | | | | | | | | |
| SEP internal flash | Non-Volatile | 1 | U14 | Flash: 512KB<br><br>Data SRAM : 256KB<br><br>Battery Powered Storage SRAM : 64B | Integrated Flash + Data SRAM + Battery Powered Storage SRAM | No | Firmware + FRU | I2C interface via iDRAC | Program write protect bit | Not user clearable |
| **2x2.5" Rear Universal Backplane** | | | | | | | | | | |
| SEP internal flash | Non-Volatile | 1 | U47 | Flash: 512KB | Integrated Flash + Data SRAM + Battery Powered | No | Firmware + FRU | I2C interface via iDRAC | Program write protect bit | Not user clearable |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Data SRAM : 256KB<br><br>Battery Powered Storage SRAM : 64B | Storage SRAM | | | | | |
| **8x EDSFF Passive Backplane** | | | | | | | | | | |
| SEP internal flash | Non-Volatile | 1 | U5 | Flash: 512KB<br><br>Data SRAM : 256KB<br><br>Battery Powered Storage SRAM : 64B | Integrated Flash + Data SRAM + Battery Powered Storage SRAM | No | Firmware + FRU | I2C interface via iDRAC | Program write protect bit | Not user clearable |
| **8x EDSFF w/ fPERC power slot Passive Backplane** | | | | | | | | | | |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---|---|---|---|---|---|---|---|---|---|---|
| SEP internal flash | Non-Volatile | 1 | U5 | Flash: 512KB<br><br>Data SRAM : 256KB<br><br>Battery Powered Storage SRAM : 64B | Integrated Flash + Data SRAM + Battery Powered Storage SRAM | No | Firmware + FRU | I2C interface via iDRAC | Program write protect bit | Not user clearable |
| **Rear X2 EDSFF Backplane** | | | | | | | | | | |
| SEP internal flash | Non-Volatile | 1 | U3 | Flash: 512KB<br><br>Data SRAM : 256KB<br><br>Battery Powered Storage | Integrated Flash + Data SRAM + Battery Powered Storage SRAM | No | Firmware + FRU | I2C interface via iDRAC | Program write protect bit | Not user clearable |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | SRAM : 64B | | | | | | |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---|---|---|---|---|---|---|---|---|---|---|
| **H965i Front PERC (Internal Controller)** | | | | | | | | | | |
| SPI Flash | Non-Volatile | 1 | U2 | 256Mb | SPI Flash | No | Card firmware | Pre-programmed before assembly. Can be updated using Dell/Broadcom tools | Not write protected. Not visible to Host Processor | User cannot clear the memory. |
| FRU | Non-volatile | 1 | U1019 | 2Kb | EEPROM | No | Card manufacturing information | Programmed at ICT during production. | Not write protected | User cannot clear the memory. |
| CPLD | Non-volatile | 1 | U1088 | 64kb | Flash | No | Power sequencing and Cache Offload | Controller may program data during FW update | Not write protected<br><br>Not visible to host CPU | User cannot clear this memory |
| MCU | Non-volatile | 1 | U41 | 8kB | Flash | No | PCIe Bifurcation information to system iDRAC | BMC may program data if there is an updated version packaged with iDRAC | Not write protected<br><br>Not visible to host CPU | User cannot clear this memory |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---|---|---|---|---|---|---|---|---|---|---|
| NVSRAM | Non-volatile | 1 | U1087 | 128kB | NVSRAM | No | Configuration data | ROC writes configuration data to NVSRAM | Not write protected<br><br>Not visible to host CPU | User cannot clear this memory |
| BMU | Non-Volatile | 1 | U1126 | 180KB | Integrated Flash + EEPROM | No | Battery Management control | ROC may program data during FW and during boot | Not write protected | User cannot clear this memory |
| SPD | Non-volatile | 1 | U22 | 256b | EEPROM | No | Memory configuration data | Pre-programmed before assembly | No write protected. Not visible to Host Processor | User cannot clear the memory. |
| NAND Flash | Non-volatile | 1 | U1100 | 512Gb | ONFI Flash | No | Cache offload during unexpected power loss | Programmed by ROC during cache offload | No write protected. Not visible to Host Processor | User cannot clear the memory. |
| SDRAM | Volatile | 9 | U1077~U1086 | 8GB | SDRAM | No | Cache for HDD I/O | ROC writes to this memory - using it as cache for data IO to HDDs | No write protected. Not visible to Host Processor | Cache can be cleared by powering off the card |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---|---|---|---|---|---|---|---|---|---|---|
| **H755 Front PERC (Internal Controller)** | | | | | | | | | | |
| SDRAM | Volatile | 9 | U1077~U1085 | 8GB | SDRAM | No | Cache for HDD I/O | ROC writes to this memory - using it as cache for data IO to HDDs | no write protected. Not visible to Host Processor | Cache can be cleared by powering off the card |
| NV Flash | Non-volatile | 1 | U1100 | 512Gb | SPI Flash | No | Card firmware | Pre-programmed before assembly. Can be updated using Dell/LSI tools | no write protected. Not visible to Host Processor | User cannot clear the memory. |
| BMU | Non-Volatile | 1 | U1126 | 180KB | Integrated Flash + EEPROM | No | Battery Management Control | ROC may program data during FW and during boot during battery detection | Not write protected<br><br>Not visible to host CPU | User cannot clear this memory |
| SPI Flash | Non-Volatile | 1 | U1086 | 128Mb | SPI Flash | No | Holds cache data during power loss | FPGA backs up DDR data to this device in case of a power failure | no write protected. Not visible to Host Processor | Flash can be cleared by powering up the card and allowing the controller to flush the contents to VDs. If the VDs are no longer available, cache can be |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | cleared by going into controller BIOS and selecting Discard Preserved Cache. |
| NVSRAM | Non-volatile | 1 | U1087 | 128KB | NVSRAM | No | Configuration data | ROC writes configuration data to NVSRAM | no write protected. Not visible to Host Processor | User cannot clear the memory. |
| FRU | Non-volatile | 1 | U1019 | 2Kb | EEPROM | No | Card manufacturing information | Programmed at ICT during production. | no write protected | User cannot clear the memory. |
| SPD | Non-volatile | 1 | U22 | 2Kb | EEPROM | No | Memory configuration data | Pre-programmed before assembly | no write protected. Not visible to Host Processor | User cannot clear the memory. |
| CPLD | Non-volatile | 1 | U1088 | 64kb | Flash | No | Power sequencing and Cache Offload | ROC may program data during FW update | Not write protected<br><br>Not visible to host CPU | User cannot clear this memory |
| MCU | Non-volatile | 1 | U41 | 8KB | EEPROM | No | PCIe Bifurcation information to system iDRAC | BMC may program data if there is an updated version | Not write protected<br><br>Not visible to host CPU | User cannot clear this memory |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | packaged with iDRAC | | |
| **H755 Adapter** | | | | | | | | | | |
| SDRAM | Volatile | 9 | U1077~U1085 | 8GB | SDRAM | No | Cache for HDD I/O | ROC writes to this memory - using it as cache for data IO to HDDs | no write protected. Not visible to Host Processor | Cache can be cleared by powering off the card |
| NV Flash | Non-volatile | 1 | U1100 | 512Gb | SPI Flash | No | Card firmware | Pre-programmed before assembly. Can be updated using Dell/LSI tools | no write protected. Not visible to Host Processor | User cannot clear the memory. |
| BMU | Non-Volatile | 1 | U1126 | 180KB | Integrated Flash + EEPROM | No | Battery Management Control | ROC may program data during FW and during boot during battery detection | Not write protected<br><br>Not visible to host CPU | User cannot clear this memory |
| SPI Flash | Non-Volatile | 1 | U1086 | 128Mb | SPI Flash | No | Holds cache data during power loss | FPGA backs up DDR data to this device in | no write protected. Not visible to Host Processor | Flash can be cleared by powering up the card and allowing the controller to flush the |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | case of a power failure | | contents to VDs. If the VDs are no longer available, cache can be cleared by going into controller BIOS and selecting Discard Preserved Cache. |
| NVSRAM | Non-volatile | 1 | U1087 | 128KB | NVSRAM | No | Configuration data | ROC writes configuration data to NVSRAM | no write protected. Not visible to Host Processor | User cannot clear the memory. |
| FRU | Non-volatile | 1 | U1019 | 2Kb | EEPROM | No | Card manufacturing information | Programmed at ICT during production. | no write protected | User cannot clear the memory. |
| SPD | Non-volatile | 1 | U22 | 2Kb | EEPROM | No | Memory configuration data | Pre-programmed before assembly | no write protected. Not visible to Host Processor | User cannot clear the memory. |
| CPLD | Non-volatile | 1 | U1088 | 64kb | Flash | No | Power sequencing and Cache Offload | ROC may program data during FW update | Not write protected<br>Not visible to host CPU | User cannot clear this memory |
| **H755N Front PERC (Internal Controller)** | | | | | | | | | | |
| NVSRAM | Non-volatile | 1 | U1087 | 128KB | NVSRAM | No | Configuration data | ROC writes configuration | No write protected. Not | User cannot clear the memory. |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | data to NVSRAM | visible to Host Processor | |
| FRU | Non-volatile | 1 | U1019 | 2Kb | EEPROM | No | Card manufacturing information | Programmed at ICT during production. | No write protected | User cannot clear the memory. |
| SPD | Non-volatile | 1 | U1019 | 2Kb | EEPROM | No | Memory configuration data | Pre-programmed before assembly | No write protected. Not visible to Host Processor | User cannot clear the memory. |
| NV Flash | Non-volatile | 1 | U1100 | 512Gb | SPI Flash | No | Card firmware | Pre-programmed before assembly. Can be updated using Dell/LSI tools | No write protected. Not visible to Host Processor | User cannot clear the memory. |
| CPLD | Non-volatile | 1 | U1088 | 64kb | Flash | No | Power sequencing and Cache Offload | NA | NA | NA |
| SPI Flash | Non-Volatile | 1 | U1086 | 128Mb | SPI Flash | No | Holds cache data during power loss | FPGA backs up DDR data to this device in case of a power failure | No write protected. Not visible to Host Processor | Flash can be cleared by powering up the card and allowing the controller to flush the contents to VDs. If the VDs are no longer available, cache can be cleared by going into |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | controller BIOS and selecting Discard Preserved Cache. |
| SDRAM | Volatile | 9 | U1077~U1085 | 8GB | SDRAM | No | Cache for HDD I/O | ROC writes to this memory - using it as cache for data IO to HDDs | No write protected. Not visible to Host Processor | Cache can be cleared by powering off the card |
| MCU | Non-volatile | 1 | U41 | 8KB | EEPROM | No | PCIe Bifurcation information to system iDRAC | NA | NA | NA |
| BMU | Non-Volatile | 1 | U1126 | 180KB | NA | No | Battery Management control | NA | NA | NA |
| **HBA355i Front (Internal Controller)** | | | | | | | | | | |
| SPI Flash | Non-Volatile | 1 | U2 | 128Mb | SPI Flash | No | Card firmware | Pre-programmed before assembly. Can be updated using Dell/LSI tools | Not write protected. Not visible to Host Processor | User cannot clear the memory. |
| FRU | Non-volatile | 1 | U5 | 2Kb | EEPROM | No | Card manufacturing information | Programmed at ICT during production. | Not write protected | User cannot clear the memory. |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---|---|---|---|---|---|---|---|---|---|---|
| CPLD | Non-volatile | 1 | U23 | 24kb | Flash | No | Power sequencing and Cache Offload | Controller may program data during FW update | Not write protected<br><br>Not visible to host CPU | User cannot clear this memory |
| MCU | Non-volatile | 1 | U41 | 8kB | EEPROM | No | PCIe Bifurcation information to system iDRAC | BMC may program data if there is an updated version packaged with iDRAC | Not write protected<br><br>Not visible to host CPU | User cannot clear this memory |
| **H355 Front PERC (Internal Controller)** | | | | | | | | | | |
| SPI Flash | Non-Volatile | 1 | U2 | 128Mb | SPI Flash | No | Card firmware | Pre-programmed before assembly. Can be updated using Dell/LSI tools | Not write protected. Not visible to Host Processor | User cannot clear the memory. |
| FRU | Non-volatile | 1 | U5 | 2Kb | EEPROM | No | Card manufacturing information | Programmed at ICT during production. | Not write protected | User cannot clear the memory. |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---|---|---|---|---|---|---|---|---|---|---|
| CPLD | Non-volatile | 1 | U23 | 24kb | Flash | No | Power sequencing and Cache Offload | Controller may program data during FW update | Not write protected<br><br>Not visible to host CPU | User cannot clear this memory |
| MCU | Non-volatile | 1 | U41 | 8kB | EEPROM | No | PCIe Bifurcation information to system iDRAC | BMC may program data if there is an updated version packaged with iDRAC | Not write protected<br><br>Not visible to host CPU | User cannot clear this memory |
| NVSRAM | Non-volatile | 1 | U3 | 128kB | NVSRAM | No | Configuration data | ROC writes configuration data to NVSRAM | Not write protected<br><br>Not visible to host CPU | User cannot clear this memory |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---|---|---|---|---|---|---|---|---|---|---|
| **Status LED Control Panel** | | | | | | | | | | |
| Microcontroller | Non-Volatile | 1 | U_TINY | 8KB | Flash | No | Driving Health and Status LED | I2C via iDRAC | Hardware strapping | User cannot clear the memory. |
| **Standard/LC RIO** | | | | | | | | | | |
| MCU | Non-Volatile | 1 | U6 | 8kB | Flash ROM | No | Standard/LC RIO Information | The data is flash via iDRAC auto update | No write protected. Not visible to Host Processor | User cannot clear the memory. |
| **TPM** | | | | | | | | | | |
| Trusted Platform Module (TPM) | Non-Volatile | 1 | U2 | 128 Bytes | EEPROM | Yes | Storage of encryption keys | Using TPM Enabled operating systems | SW write protected | F2 Setup option |
| **Power Button Control Panel** | | | | | | | | | | |
| SPI Flash | Non-Volatile | 1 | U2 | 32 Mb | SPI Flash | No | EasyRestore functionality contains Service Tag, Copy of SEL logs | SPI interface from iDRAC to Right Cntl Panel | Embedded iDRAC subsystem firmware actively controls sub area based write protection as needed. | The user cannot clear memory. |
| **LOM** | | | | | | | | | | |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---|---|---|---|---|---|---|---|---|---|---|
| SPI Flash | Non-Volatile | 1 | U1 | 8-Mbit DataFlash (with Extra 256-Kbits) | SPI Flash EEPROM | Yes | Firmware, configuration data | Firmware and some configuration data flashed via Dell Update Package (DUP); some configuration data is programmed during manufacturing ; end user configuration data is written via UEFI HII | Reserving write protection function for HW design. | User cannot clear the memory. |
| MCU | Non-Volatile | 1 | U2 | 64KB Flash and 8KB of SRAM | Flash ROM | No | LOM Security data | Off-line programming Before production | No write protected. Not visible to Host Processor | User cannot clear the memory |
| **BOSS-N1** | | | | | | | | | | |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---|---|---|---|---|---|---|---|---|---|---|
| RAID controller external SPI FLASH | Non-Volatile | 1 | U17 | 8Mb | FLASH EEPROM | No | Boot code, FW | By programming the image via firmware update process | N/A | Use Flash tool, type “go.nsh w y” |
| CPLD | Non-Volatile | 1 | U1120 | 256Kb | | | | | | |
| MCU | Non-volatile | 1 | U1113 | 8KB | | | | | | |
| FRU | Non-Volatile | 1 | U_BOSS_EEPROM | 2Kb | FLASH EEPROM | No | Card manufacturing information | During Manufacturing, by programming the image via firmware update process. During runtime, by | N/A | By writing to Flash |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | I2C Proprietary Command Protocol | | |
| **Quick Sync 2** | | | | | | | | | | |
| MCU | Non-volatile | 1 | USAM7 | 2048kB | Flash ROM | No | Driving Health/ Status LED and Wifi-BT communication. | SPI interface via iDRAC | Hardware strapping | User cannot clear the memory. |
| **R2A/R3A/ R1P/R2S/R3P/R3R/R3S/R4P** | | | | | | | | | | |
| MCU | Non-volatile | 1 | U1 | 8kB | Flash ROM | No | Riser information | The data is flash via iDRAC auto update | No write protected. Not visible to Host Processor | User cannot clear the memory. |
| **R2Q/R3Q/R2P/R2R** | | | | | | | | | | |
| MCU | Non-volatile | 2 | U1 | 8kB | Flash ROM | No | Riser information | The data is flash via iDRAC auto update | No write protected. Not visible to Host Processor | User cannot clear the memory. |
| **PUCK_50A** | | | | | | | | | | |
| MCU | Non-volatile | 1 | U1 | 16kB | Flash ROM | No | PUCK information | The data is flash via iDRAC auto update | No write protected. Not visible to Host Processor | User cannot clear the memory. |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---|---|---|---|---|---|---|---|---|---|---|
| **PSU** | | | | | | | | | | |
| **DELTA PSU (700W, 800W, 1100W, 1400W, 1800W)** | | | | | | | | | | |
| Primary MCU | Non-volatile | 1 | IC703 | 64KB | Internal Flash | No | Boot code, FW | The data is flash via Dell Update Package (DUP) | SW write protected | Before firmware update, the memory will be cleared. |
| Secondary MCU | Non-volatile | 1 | IC805 | 64KB | Internal Flash | No | Boot code, FW | The data is flash via Dell Update Package (DUP) | SW write protected | Before firmware update, the memory will be cleared. |
| FRU | Non-volatile | 1 | IC704 | 16KB | EEPROM | No | PSU information | During Manufacturing, by programming the image via firmware update process | SW write protected | User cannot clear the memory. |
| **ARTESYN PSU (800W, 1100W, 1400W)** | | | | | | | | | | |
| Primary MCU | Non-volatile | 1 | U317 (TI) | 64K | Internal Flash | No | Boot code, FW | The data is flash via Dell Update Package (DUP) | SW write protected | Before firmware update, the memory will be cleared. |

| Item | Non-Volatile or Volatile | Quantity | Reference Designator | Size | Type (e.g. Flash PROM, EEPROM) | Can user programs or operating system write data to it during normal operation? | Purpose? (e.g. boot code) | How is data input to this memory? | How is this memory write protected? | How is the memory cleared? |
|---|---|---|---|---|---|---|---|---|---|---|
| Secondary MCU | Non-volatile | 2 | U301 (TI )<br>U315 (ST ) | 32K<br>128K | Internal Flash | No | Boot code, FW | The data is flash via Dell Update Package (DUP) | SW write protected | Before firmware update, the memory will be cleared. |
| FRU | Non-volatile | 1 | U305 | 2Mb | SERIAL FLASH | No | PSU information | During Manufacturing | SW write protected | User cannot clear the memory. |
| **LiteOn PSU (700W, 800W, 1100W, 1400W, 1800W)** | | | | | | | | | | |
| Primary MCU | Non-volatile | 1 | IC050 | 64K | Internal Flash | No | Boot code, FW | The data is flash via Dell Update Package (DUP) | SW write protected | Before firmware update, the memory will be cleared. |
| Secondary MCU/FRU | Non-volatile | 1 | IC900 | 128K | Internal Flash | No | Boot code, FW | The data is flash via Dell Update Package (DUP) | SW write protected | Before firmware update, the memory will be cleared. |

**NOTE:** For any information that you may need, direct your questions to your Dell Marketing contact.

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