ATGBICS® by APPROVED TECHNOLOGY

Technical Datasheet

OSFP-800G-SR8

800GBase OSFP SR8 Transceiver

Hot Pluggable, +3.3V, Dual MPO, 850nm, MMF, 50m, Commercial Temperature

FEATURES

- OSFP Serial Optical Interface
  - 8x100G PAM4 retimed 800GAUI-8 electrical interface
  - MPO16 APC connector are provided
  - 8 channel VCSEL arrays and 8 channels PIN photo detector arrays
  - Maximum link length of 60m on OM3 or 100m on OM4
- Supports both 800GBASE-SR8 800G Ethernet
- OSFP MSA Compliant
  - Hot Pluggable OSFP form factor
  - Compliant to OSFP Module Specification Rev 5.0
  - Compliant with CMIS 5.2
- Support Protocol
  - Compliant with IEEE 802.3db
  - Compliant to IEEE 802.3ck
- Low Power Consumption
- Commercial Operating Temperature Range: 0 to 70ºC

APPLICATIONS

- 800GBase-SR8 800G Ethernet
- Data Centre

DESCRIPTION

OSFP-800G-SR8 is an Eight-Channel, Parallel, Pluggable, Fibre-Optic OSFP for 800 Gigabit Ethernet applications. This transceiver is a high performance module for short-range data communication and interconnect application. It integrates eight data lanes in each direction with 8x53.125GBd. The length of OSFP SR8 is up to 60 meters over OM3 MMF or 100 meters over OM4 MMF. This module is designed to operate over multimode fibre systems using a nominal wavelength of 850nm.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Ts	-40	85	ºC
Case Operating Temperature	Top	0	70	ºC
Relative Humidity (non-condensing)	RH	15	85	%
Supply Voltage	Vcc	-0.5	3.6	V
Receiver Damage Threshold, per Lane	PRdmg	5		dBm

RECOMMENDED OPERATING ENVIRONMENT

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Operating Case Temperature	Top	0		70	ºC	
Relative Humidity (non-condensing)	RH	15		85	%	
Power Supply Voltage	Vcc	3.135		3.465	V	
Total Power Consumption	Pc	-		16	W	1
Supply Current per end				5.1	A	
Bit Rate	BR			850	Gbps	
Fibre Length on OM3 MMF				60	m	
Fibre Length on OM4 MMF				100	m	
I2C Clock Frequency		0		1000	kHz	

Note:

1. Under condition of 3.465V operating supply voltage, and 70ºC case temperature.

OPTICAL PARAMETERS

Parameter		Symbol	Min	Typical	Max	Unit	Note
TRANSMITTER							
Data rate per lane		DR		53.125		GBd	
Modulation format				PAM4			
Centre Wavelength		λ	840	860	868	nm	1
RMS spectral width		σ			0.6	nm	
Average Launch power, each lane		Pavg	-1		4	dBm	
Optical Power OMA, each Lane,max		POMA		3.5		dBm	
OMAouter, each lane min	**max (TECQ, TDECQ) <1.8 dB**		max [-2.6, max (TECQ,TECQ) – 4.4]			dBm	
	1.8 < max (TECQ, TDECQ) < 4.4 dB						
Transmitter and dispersion eye closure (TDECQ), each lane		TDECQ			4.4	dB	
Transmitter eye closure for PAM4 (TECQ), each lane		TECQ			4.4	dB	
Extinction ratio		ER	2.5			dB	
Transmitter power excursion, each lane					2.3	dBm	
Optical Return Loss Tolerance		ORLT			14	dB	
Optical Power for TX DISABLE					-30	dBm	
Encircled flux			≥86% at 19 um ≤30% at 4.5 um				2
RECEIVER							
Data rate per lane		BR		53.125		Gbd	
Modulation format				PAM4			
Centre Wavelength		λ	842	850	948	nm	
Damage threshold			5			dBm	
Average receive power, each lane			–6.4		4	dBm	
Receive power, each lane (OMAouter)					3.5	dBm	
Receiver reflectance		Rr			–15	dB	
Receiver sensitivity, each lane			RS = max (-4.6, TECQ - 6.4)			dBm	3
Stressed receiver sensitivity, each lane					-2	dBm	
Rx LOS	**Assert**		-15			dBm	
	De-assert				-7.5	dBm	
	Hysteresis		0.5		5	dB	

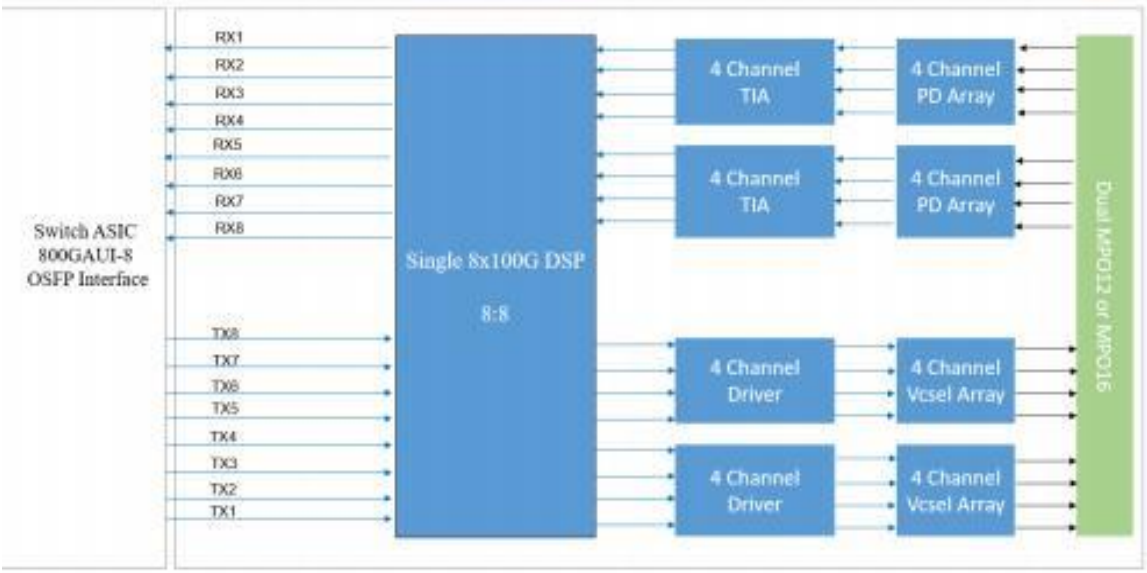
Note:

1. Defined according to the performance of the laser used.
2. Measured into type A1a.2 or type A1a.3, or A1a.4, 50 um fibre, in accordance with IEC 61280-1-4
3. Receiver sensitivity is informative and is defined for a transmitter with a value of TECQ. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC.

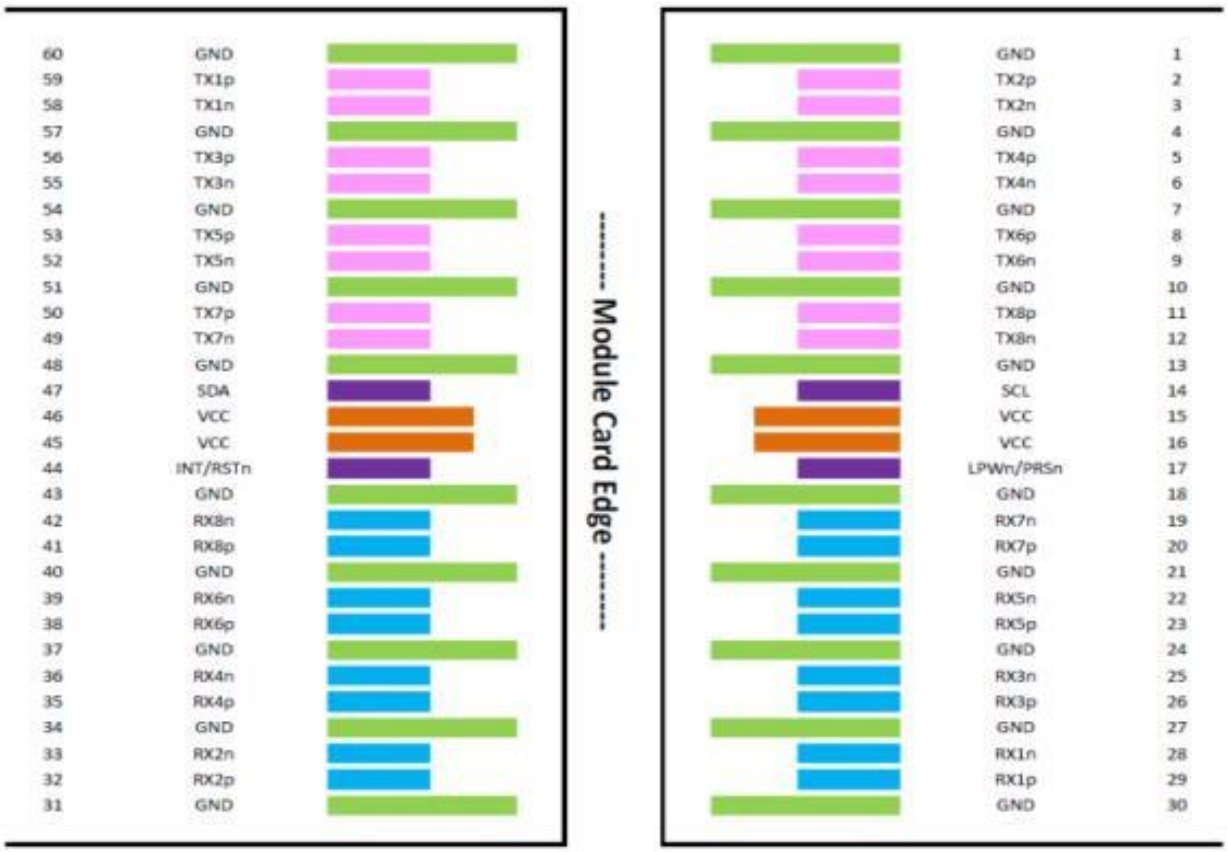
ELECTRICAL CHARACTERISTICS

Parameters	Min	Typical	Max	Unit
Pre FEC Bit Error Ratio			2.4E-4	
Post FEC Bit Error Ratio			1E-12	
TRANSMITTER (EACH LANE)				
Differential pk-pk Input Voltage tolerance	750			mV
Differential Termination Mismatch			10	%
Eye height	10			mV
Common-mode to differential-mode return loss	IEEE802.3ck Equation (120G-1)			dB
Vertical eye closure			12	dB
Effective return loss	7.3			dB
Transition Time	10			ps
RECEIVER (EACH LANE)				
Differential data output swing	300		900	mVpp
Differential termination mismatch			10	%
Eye height	15			mV
Vertical eye closure			12	dB
Common-mode to differential-mode return loss	IEEE802.3ck Equation (120G-1)			
Effective return loss	8.5			dB
Transition time	8.5			ps

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENT



OSFP Transceiver Electrical Pad Layout

Pin	Logic	Symbol	Description	Plug Sequence
1		GND	Ground	1
2	CML-I	Tx2p	Receiver Data Non-Inverted	3
3	CML-I	Tx2n	Receiver Data Inverted	3
4		GND	Ground	1
5	CML-I	Tx4p	Receiver Data Non-Inverted	3
6	CML-I	Tx4n	Receiver Data Inverted	3
7		GND	Ground	1
8	CML-I	Tx6p	Receiver Data Non-Inverted	3
9	CML-I	Tx6n	Receiver Data Inverted	3
10		GND	Ground	1
11	CML-I	TX8p	Receiver Data Non-Inverted	3
12	CML-I	TX8n	Receiver Data Inverted	3
13		GND	Ground	1
14	LVCMOS- I/O	SCL	2-wire Serial interface clock	3
15		VCC	+3.3V Power	2
16		VCC	+3.3V Power	2
17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present	3
18		GND	Ground	1
19	CML-O	RX7n	Receiver Data Inverted	3
20	CML-O	RX7p	Receiver Data Non-Inverted	3
21		GND	Ground	1
22	CML-O	RX5n	Receiver Data Inverted	3
23	CML-O	RX5p	Receiver Data Non-Inverted	3
24		GND	Ground	1
25	CML-O	RX3n	Receiver Data Inverted	3
26	CML-O	RX3p	Receiver Data Non-Inverted	3
27		GND	Ground	1
28	CML-O	RX1n	Receiver Data Inverted	3
29	CML-O	RX1p	Receiver Data Non-Inverted	3
30		GND	Ground	1
31		GND	Ground	1
32	CML-O	RX2p	Receiver Data Non-Inverted	3
33	CML-O	RX2n	Receiver Data Inverted	3
34		GND	Ground	1
35	CML-O	RX4p	Receiver Data Non-Inverted	3
36	CML-O	RX4n	Receiver Data Inverted	3

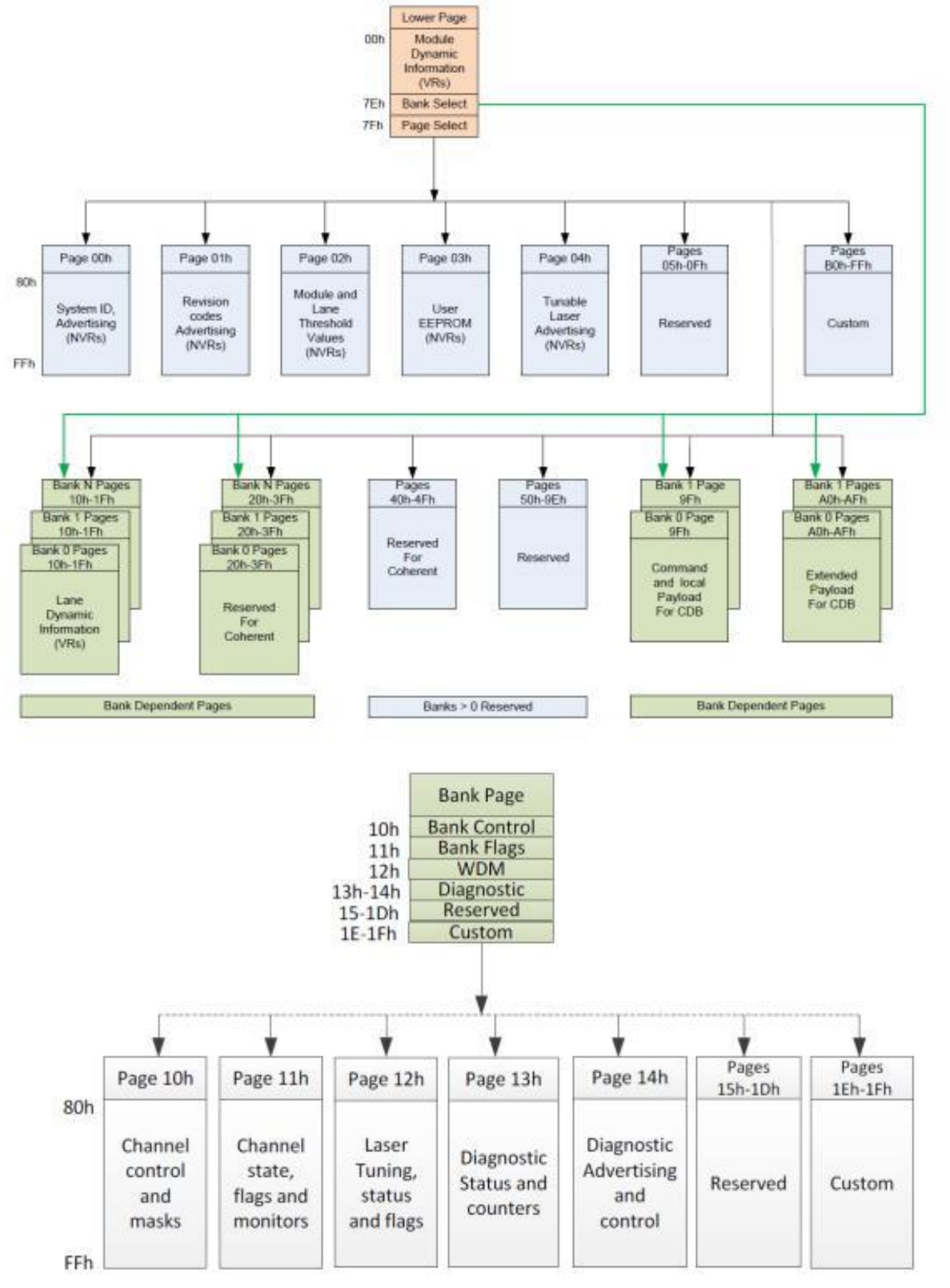
CONTINUED

37		GND	Ground	1
38	CML-O	RX6p	Receiver Data Non-Inverted	3
39	CML-O	RX6n	Receiver Data Inverted	3
40		GND	Ground	1
41	CML-O	RX8p	Receiver Data Non-Inverted	3
42	CML-O	RX8n	Receiver Data Inverted	3
43		GND	Ground	1
44	Multi-Level	INT/RSTn	Module Interrupt / Module Reset	3
45		VCC	+3.3V Power	2
46		VCC	+3.3V Power	2
47	LVCMOS- I/O	SDA	2-wire Serial interface data	3
48		GND	Ground	1
49	CML-I	TX7n	Transmitter Data Inverted	3
50	CML-I	TX7p	Transmitter Data Non-Inverted	3
51		GND	Ground	1
52	CML-I	TX5n	Transmitter Data Inverted	3
53	CML-I	TX5p	Transmitter Data Non-Inverted	3
54		GND	Ground	1
55	CML-I	TX3n	Transmitter Data Inverted	3
56	CML-I	TX3p	Transmitter Data Non-Inverted	3
57		GND	Ground	1
58	CML-I	TX1n	Transmitter Data Inverted	3
59	CML-I	TX1p	Transmitter Data Non-Inverted	3
60		GND	Ground	1

Note:

1. Plug Sequence specifies the mating sequence of the host connector and module. The contact sequence is 1,2,3.
2. LPWn/PRSn is a multi-level signal for low power control from host to module and module presence indication from module to host. It designed according to OSFP Module Specification Section 13.5.3
3. INT/RSTnisa multi-level signal for interrupt request from module to host and reset control from host to module. It designed according to OSFP Module Specification Section 13.5.2

USER INTERFACE



CMIS Module Memory Map

MULTIPLE APPLICATION SUPPORT

The OSFP-800G-SR8 supports CMIS 5.2 defined Application Advertising, Application Selection and Instantiation.

Address (Dec)	Application		Value (Hex)	Description
	AppSel Code	Name		
85	NA	Module Type encoding	1	Optical Interfaces: MMF
86	0001b	HostInterfaceID	4B	HostInterfaceIDApp1: 100GAUI-1-S C2M
87		MediaInterfaceID	D	MediaInterfaceIDApp1: 100GBASE-SR
88		HostLaneCount&MediaLaneCount	11	LaneCountApp1: TX & RX 1 lanes
89		HostLaneAssignmentOptions	FF	Permissible first host lane number: lanes 1, 2, 3, 4, 5, 6, 7, 8
01h:176		MediaLaneAssignmentOptions	FF	Permissible first media lane number: lanes 1, 2, 3, 4, 5, 6, 7, 8
90	0010b	HostInterfaceID	11	HostInterfaceIDApp2:400GAUI-8
91		MediaInterfaceID	10	MediaInterfaceIDApp2:400GBASE-SR8
92		HostLaneCount&MediaLaneCount	88	LaneCountApp2: TX & RX 8 lanes
93		HostLaneAssignmentOptions	1	Permissible first host lane number: lane 1
01h:177		MediaLaneAssignmentOptions	1	Permissible first media lane number: lane 1
94	0011b	HostInterfaceID	E	HostInterfaceIDApp3:200GAUI-8 C2M
95		MediaInterfaceID	0	MediaInterfaceIDApp3:200GBASE-SR8(SFF-8024 Undefined)
96		HostLaneCount&MediaLaneCount	88	LaneCountApp3: TX & RX 8 lanes
97		HostLaneAssignmentOptions	1	Permissible first host lane number: lane 1
01h:178		MediaLaneAssignmentOptions	1	Permissible first media lane number: lane 1
98	0100b	HostInterfaceID	51	HostInterfaceIDApp4:800G S C2M
99		MediaInterfaceID	12	MediaInterfaceIDApp4:800G-SR8
100		HostLaneCount&MediaLaneCount	88	LaneCountApp4: TX & RX 8 lanes
101		HostLaneAssignmentOptions	1	HostLaneAssignmentOptionsApp4: begin lane 1
01h:179		MediaLaneAssignmentOptions	1	Permissible first media lane number: lane 1
102	0101b	HostInterfaceID	4F	HostInterfaceIDApp5:400GAUI-4-S C2M
103		MediaInterfaceID	11	MediaInterfaceIDApp5:400GBASE-SR4
104		HostLaneCount&MediaLaneCount	44	LaneCountApp5: TX & RX 4 lanes
105		HostLaneAssignmentOptions	11	Permissible first host lane number: lane 1, 5
01h:180		MediaLaneAssignmentOptions	11	Permissible first media lane number: lane 1,5
106	0110b	HostInterfaceID	4D	HostInterfaceIDApp6:200GAUI-2-S C2M
107		MediaInterfaceID	1B	MediaInterfaceIDApp6:200GBASE-SR2
108		HostLaneCount&MediaLaneCount	22	LaneCountApp6: TX & RX 2 lanes
109		HostLaneAssignmentOptions	55	Permissible first host lane number: lanes 1, 3, 5, and 7
01h:181		MediaLaneAssignmentOptions	55	Permissible first media lane number: lanes 1, 3, 5, and 7
110			FF	HostInterfaceIDApp7
111			0	MediaInterfaceIDApp7
112			0	LaneCountApp7
113			0	HostLaneAssignmentOptionsApp7
114			0	HostInterfaceIDApp8
115			0	MediaInterfaceIDApp8
116			0	LaneCountApp8
117			0	HostLaneAssignmentOptionsApp8

The OSFP-800G-SR8 supports 6 applications:

- 800GBASE-SR8
- 400GBASE-SR8
- 200GBASE SR8
- 2X400GBASE-SR4
- 4X200GBASE-SR2
- 8X100GBASE-SR1

The host can select applications by programming the AppSel value in Staged Set 0.

AppSel=1 is the default application populated in the Active Control Set at power-on or reset.

Note that the channels of the module are independent and can be configured separately (ie. up to eight 100GBASE-SR instances can be configured). However, it does not support different applications with different channels at the same time. OSFP-800G-SR8 supports two methods of application selection and instantiation. The first method is implemented according to CMIS, and the second method is customized, which is simpler.

First method:

The applications switching configuration sequence is as follows: read Application Descriptor Registers and select the required Appsel. Write application configuration to DPConfigLane<i>

in Stage Control Set 0, then write 1 to ApplyDPInitLane<i> to trigger Application Instantiation.

The Active Set can be read from page11h.

For example, select AppDescriptor3:

Step 1: Write 0x30 in Page10h Byte145~Byte152(8 bytes)—Set AppselCode3

Step 2: Write 0xFF in Page10h Byte143—Set trigger register to run Application Instantiation.

Second method:

Set the value of Page10h Byte240. This is a private definition.

Code Value	Bit Pattern	Host Electrical Interface	Media Interface
0	00000000b	100GAUI-1-S C2M	100GBASE-SR1
1	00000001b	400GAUI-8	400GBASE-SR8
2	00000010b	200GAUI-8	200GBASE-SR8
3	00000011b	800G S C2M	800G-SR8
4	00000100b	400GAUI-4-S C2M	400GBASE-SR4
5	00000101b	200GAUI-2-S C2M	200GBASE-SR2

Private Host Electrical Interface Codes

TX & RX SQUELCH

Default Tx and Rx auto-squelch is enabled, but Tx and Rx auto squelch disable, and force squelching function are not supported.

TX INPUT EQUALISATION

Default Tx adaptive equalization is enabled, but Tx adaptive equalization disable, and fixed equalisation adjust function are not supported.

RX OUTPUT EQUALISATION

Rx output Equalization follows CMIS Table 6-7, with default 1dB, readable and writable

Table 6-7 Rx Output Equalization Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000b	0dB (No Equalization)	0dB (No Equalization)
1	0001b	1 dB	0.5 dB
2	0010b	2 dB	1.0 dB
3	0011b	3 dB	1.5 dB
4	0100b	4 dB	2.0 dB
5	0101b	5 dB	2.5 dB
6	0110b	6 dB	3.0 dB
7	0111b	7 dB	3.5 dB
8-10	1000b-1010b	**Reserved**	**Reserved**
11-15	1011b-1111b	Custom	Custom

RX Output Equalisation code table

RX OUTPUT AMPLITUDE

Rx output amplitude follows CMIS Table 6-8, Rx output amplitude is the difference peak-to-peak EYE high when Rx output equalization is set to 0dB. The default value of output amplitude is set to 2, with typical differential 600mVp-p.

Table 6-8 Rx Output Amplitude Codes

Code Value	Bit pattern	Output Amplitude
0	0000b	100-400 mV (P-P)
1	0001b	300-600 mV (P-P)
2	0010b	400-800 mV (P-P)
3	0011b	600-1200 mV (P-P)
4-14	0100b-1110b	**Reserved**
15	1111b	Custom

RX Output Equalisation code table

LOOPBACK CAPABILITIES

Media side input loopback and Host side input loopback feature are supported, loopback control method refers to CMIS.

Byte	Bits	Field Name	Field Description
13h:128	6	Simultaneous Host and Media Side loopbacks	0b: not supported
	5	Per Lane Media Side Loopbacks	1b: supported
	4	Per Lane Host Side Loopbacks	1b: supported
	3	Host Side Input Loopback	1b: supported
	2	Host Side Output Loopback	1b: supported
	1	Media Side Input Loopback	1b: supported
	0	Media Side Output Loopback	1b: supported

OSFP Rx Output Equalisation code table

DIGITAL DIAGNOSTIC MONITOR ACCURACY

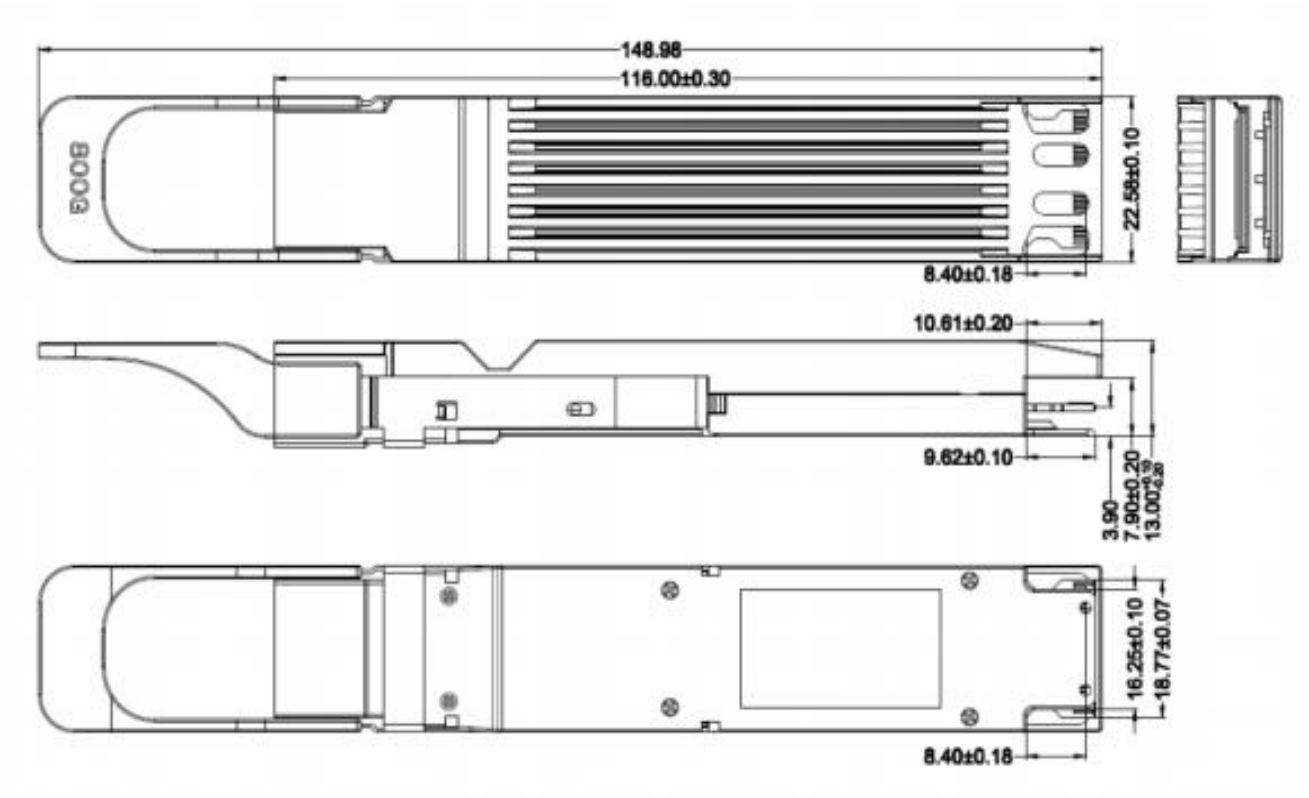
The following characteristics are defined over recommended operating conditions

Parameter	Accuracy	Unit	Note
Internally measured transceiver temperature	+/-3		1
Internally measured transceiver supply voltage	+/-3	%	
Measured Tx bias current	+/-10	%	
Measured Tx output power	+/-3	dB	2
Measured Rx received average optical power	+/-3	dB	

Note:

1. Test point is the hotspot of the module.
2. DDM reports stability within 0.5 dB when temperature is stable. TX DDM reports -40 dBm when TX disable.

MECHANICAL DIMENSIONS (UNIT: mm)



Package Dimensions (specified in OSFP MSA)

LASER SAFETY & ELECTROMAGNETIC COMPATIBILITY

The OSFP-800G-SR8 are Class 1 Laser products according to FDA/CDRH, IEC-60825-1 and IEC60825-2 standards. They must be operated under the specified operating conditions. They are designed to meet FCC Class B limits.