ATGBICS® by APPROVED TECHNOLOGY

Technical Datasheet

OSFP-400G-SR4-100-IB

400G OSFP SR4 InfiniBand Transceiver

Hot Pluggable, +3.3V, MPO-12, 850nm, MMF, 100m, Commercial Temperature

FEATURES

- Hot-pluggable OSFP form factor
- VCSEL transmitter and PIN PD receiver
- Support 425Gb/s aggregate bit rate
- Support both 4x100G Ethernet and InfiniBand NDR
- Compliant with IEEE 802.3-2022: 4x100GBASE-VR1 optical interface
- Compliant with IEEE 802.3ck-2022: 4x100GAUI-1 C2M electrical interface
- Compliant with InfiniBand Trade Association (IBTA)Specification 1.6: InfiniBand NDR electrical and optical interface
- Compliant with OSFP MSA Specification Rev 5.0 RHS housing (with the longer body:107.8mm) with MPO-12/APC receptacle
- Compliant with CMIS Rev 5.0
- Power dissipation < 9W
- Two wire serial Interface with digital diagnostic monitoring
- Complies with EU Directive 2011/65/EU (RoHS compliant)
- Class 1 Laser
- Commercial Operating Temperature Range: 0 to 70°C

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	85	ºC
Supply Voltage	V_{CC}	-0.5	3.6	V
Relative Humidity (non-condensing)	RH	5	85	%
Data Input Voltage Differential	$\lvert V_{DIP}-V_{DIN}\rvert$	-	1	V
Control Input Voltage	V_I	-0.3	V_{CC}+0.5	V
Control Output Current	I_O	-20	20	mA

RECOMMENDED OPERATING ENVIRONMENT

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Operating Case Temperature	T_{OPR}	0	-	70	ºC	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	I_{CC_IP}	-	-	3600	mA	
Sustained peak current at hot plug	I_{CC_SP}	-	-	2997	mA	
Maximum Power Dissipation	P_D	-	-	9	W	
Maximum Power Dissipation, Low Power Mode	P_{DLP}	-	-	2	W	
Signalling Speed per Lane	DRL	-	53.125	-	GBd	
Control Input Voltage High	V_{IH}	V_{CC}*0.7	-	V_{CC}+0.3	V	
Control Input Voltage Low	V_{IL}	-0.3	-	V_{CC}*0.3	V	
Two Wire Serial Interface Clock Rate	-	-	-	400	kHz	
Power Supply Noise 1 kHz - 1 MHz (p-p)	-	-	-	66	mVpp	
Operating Distance	-	2	-	100	m	

OPTICAL PARAMETERS

Parameter	Symbol	Min	Typical	Max	Unit	Notes
TRANSMITTER						
Signalling Rate, each lane (range)	-	53.125 ± 100 ppm			GBd	
Wavelength	λC	844	850	860	nm	
RMS spectral width	RMS	-	-	0.65	dB	1
Average Launch Power, each lane	AOPL	-4.6	-	4	dBm	
Outer Optical Modulation Amplitude (OMAouter), each lane for max (TECQ, TDECQ) <= 1.8 dB for 1.8 < max (TECQ, TDECQ) <= 4.4 dB	OMAouter	-2.6 -4.4+max (TECQ, TDECQ)	-	3.5	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	-	-	4.4	dB	
Transmitter eye closure for PAM4 (TECQ), each lane	TECQ	-	-	4.4	dB	
Over/under-shoot	-	-		29	%	
Transmitter power excursion, each lane	-	-		2.3	dBm	
Average Launch Power of OFF Transmitter, each lane	TOFF	-	-	-30	dBm	
Extinction Ratio, each lane	ER	2.5	-	-	dB	
Transmitter transition time, each lane	Tr	-	-	17	ps	
RIN14OMA	RIN	-	-	-132	dB/Hz	
Optical return loss tolerance	ORL	-	-	14	dB	
Encircled Flux	-	>=86% at 19 μm <=30% at 4.5 μm				
RECEIVER						
Signalling Rate, each lane (range)	-	53.125 ± 100 ppm			GBd	
Wavelength	λC0	840	-	860	nm	
Damage Threshold, each Lane	AOPD	5	-	-	dBm	
Average Receive Power, each Lane	AOPR	-6.3	-	4	dBm	
Receive Power (OMAouter), each Lane	OMAR	-	-	3.5	dBm	
Receiver Reflectance	RR	-	-	-15	dB	
Receiver sensitivity (OMAouter) for TECQ < 1.4 dB for 1.4 dB <=TECQ<=3.4 dB	SOMA	-	-	-4.4 -6.2 + TECQ	dBm	
Stressed Receiver Sensitivity (OMAouter), each Lane	SRS	-	-	-1.8	dBm	2
CONDITIONS OF STRESSED RECEIVER SENSITIVITY TEST						
Stressed eye closure for PAM4 (SECQ), lane under test	SECQ	-	4.4	-	dB	
OMAouter of each aggressor lane	-	-	3.5	-	dBm	

Note:

1. RMS spectral width is the standard deviation of the spectrum
2. Measured with conformance test signal at TP3 for the BER = $2.4x10^{-4}$

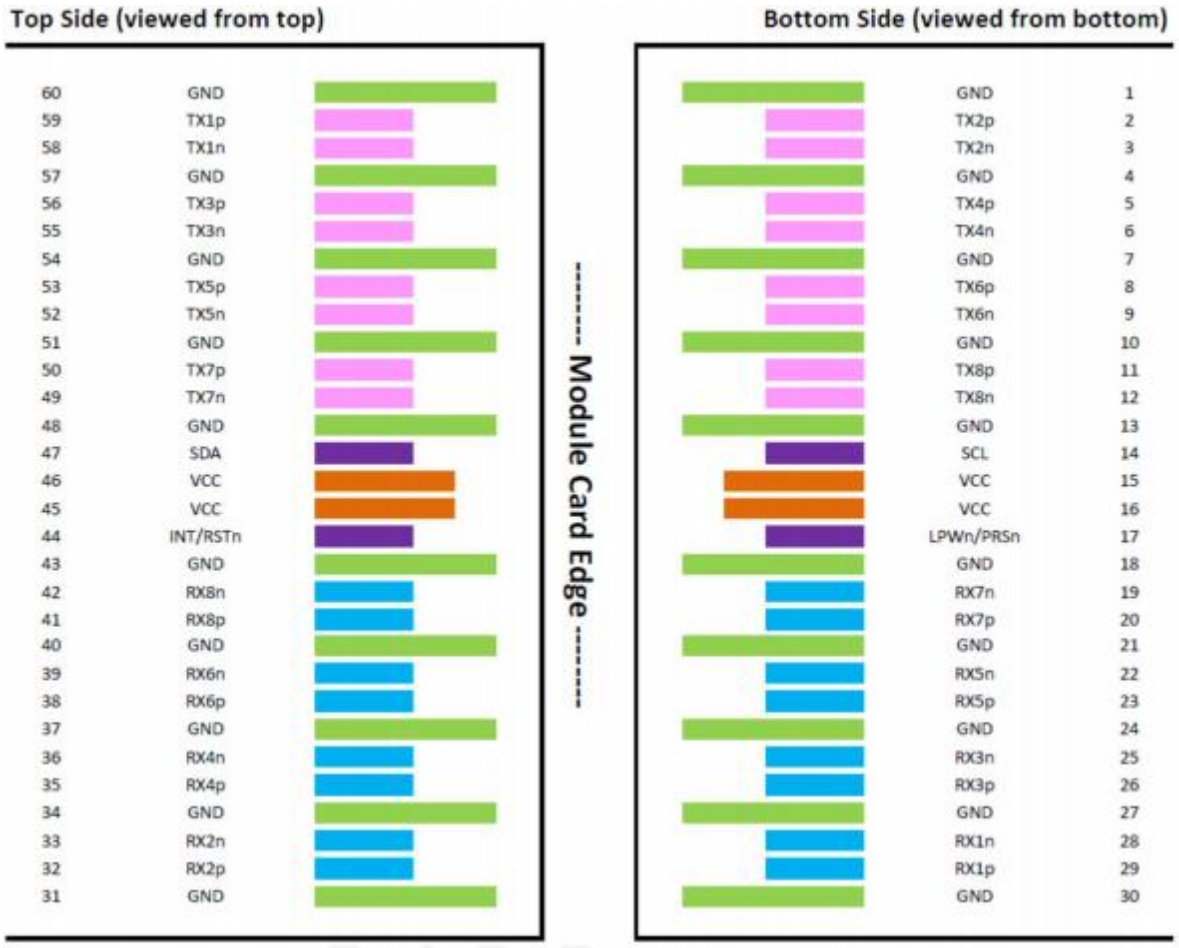
ELECTRICAL CHARACTERISTICS (High Speed Signal)

Parameter	Symbol	Min	Typical	Max	Unit	Note
TRANSMITTER (Module Input, TP1)						
Differential pk-pk input Voltage tolerance (TP1a)	-	750	-	-	mV	
Peak-to-peak AC common-mode voltage tolerance **Low-frequency, VCMLF** **Full-band, VCMFB**	-	 32 80	-	-	mV	
Differential-mode to common-mode return loss	RLcd	802.3ck 120G-2			dB	
Effective return loss	ERL	8.5	-	-	dB	
Differential termination mismatch	-	-	-	10	%	
Single-ended voltage tolerance range	-	-0.4	-	3.3	V	
DC common-mode voltage tolerance	-	-0.35	-	2.85	V	
RECEIVER (Module Output, TP4)						
Peak-to-peak AC common-mode voltage **Low-frequency, VCMLF** **Full-band, VCMFB**	-	-	-	 32 80	mV	
Differential peak-to-peak output voltage **Short mode** **Long mode**	-	-	-	 600 845	mV	
Eye height	EH	15	-	-	mV	
Vertical eye closure	VEC	-	-	12	dB	
Common-mode to differential-mode return loss	RLDc	802.3ck 120G-1			dB	
Effective return loss	ERL	8.5	-	-	dB	
Differential termination mismatch	-	-	-	10	%	
Transition time	-	8.5	-	-	ps	
DC common-mode voltage tolerance	-	-0.35	-	2.85	V	

ELECTRICAL CHARACTERISTICS (Low Speed Control and Sense Signals)

Parameter	Symbol	Min.	Max.	Unit
Module output SCL and SDA	V_{OL}	0	0.4	V
Module Input SCL and SDA	V_{IL}	-0.3	V_{CC}*0.3	V
	V_{IH}	V_{CC}*0.7	V_{CC}+0.5	V
INT/RSTn	Comply with OSFP MSA 5.0 Table 13-4			

PIN ASSIGNMENT



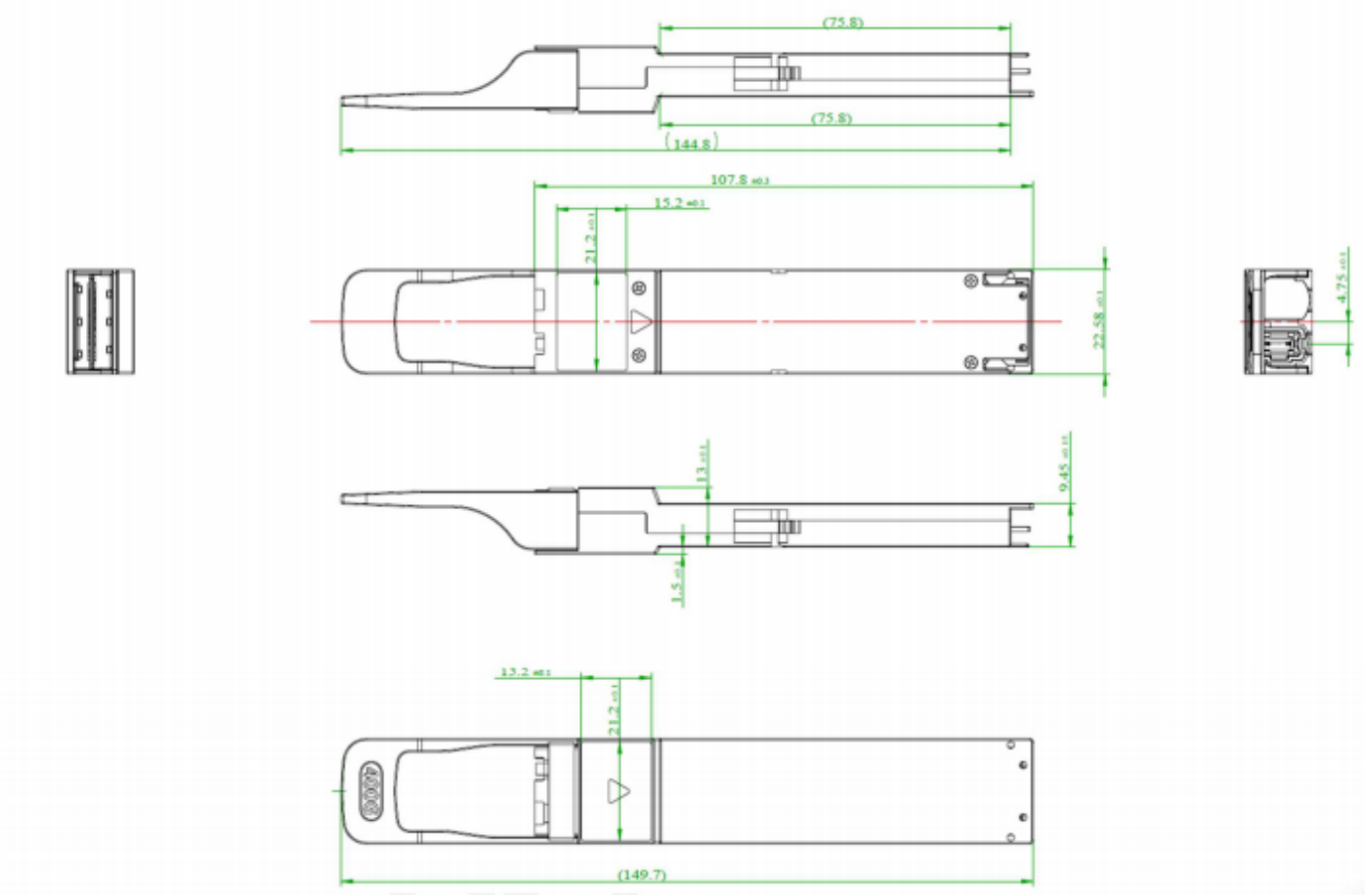
Pinout definitions of OSFP module inputs/outputs

Pin	Logic	Symbol	Description	Note	Pin	Logic	Symbol	Description	Note
1		GND	Ground		**31**		GND	Ground	
2	CML-I	TX2p	Transmitter Data Non-Inverted		**32**	CML-O	RX2p	Receiver Data Non-Inverted	
3	CML-I	TX2n	Transmitter Data Inverted		**33**	CML-O	RX2n	Receiver Data Inverted	
4		GND	Ground		**34**		GND	Ground	
5	CML-I	TX4p	Transmitter Data Non-Inverted		**35**	CML-O	RX4p	Receiver Data Non-Inverted	
6	CML-I	TX4n	Transmitter Data Inverted		**36**	CML-O	RX4n	Receiver Data Inverted	
7		GND	Ground		**37**		GND	Ground	
8	CML-I	TX6p	Transmitter Data Non-Inverted	1	**38**	CML-O	RX6p	Receiver Data Non-Inverted	1
9	CML-I	TX6n	Transmitter Data Inverted	1	**39**	CML-O	RX6n	Receiver Data Inverted	1
10		GND	Ground		**40**		GND	Ground	
11	CML-I	TX8p	Transmitter Data Non-Inverted	1	**41**	CML-O	RX8p	Receiver Data Non-Inverted	1
12	CML-I	TX8n	Transmitter Data Inverted	1	**42**	CML-O	RX8n	Receiver Data Inverted	1
13		GND	Ground		**43**		GND	Ground	
14	LVCMOS-I/O	SCL	2-wire Serial interface clock		**44**	Multi-Level	INT/RST n	Module Interrupt / Module Reset	
15		VCC	+3.3V Power		**45**		VCC	+3.3V Power	
16		VCC	+3.3V Power		**46**		VCC	+3.3V Power	
17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present		**47**	LVCMOS-I/O	SDA	2-wire Serial interface data	
18		GND	Ground		**48**		GND	Ground	
19	CML-O	RX7n	Receiver Data Inverted	1	**49**	CML-I	TX7n	Transmitter Data Inverted	1
20	CML-O	RX7p	Receiver Data Non-Inverted	1	**50**	CML-I	TX7p	Transmitter Data Non-Inverted	1
21		GND	Ground		**51**		GND	Ground	
22	CML-O	RX5n	Receiver Data Inverted	1	**52**	CML-I	TX5n	Transmitter Data Inverted	1
23	CML-O	RX5p	Receiver Data Non-Inverted	1	**53**	CML-I	TX5p	Transmitter Data Non-Inverted	1
24		GND	Ground		**54**		GND	Ground	
25	CML-O	RX3n	Receiver Data Inverted		**55**	CML-I	TX3n	Transmitter Data Inverted	
26	CML-O	RX3p	Receiver Data Non-Inverted		**56**	CML-I	TX3p	Transmitter Data Non-Inverted	
27		GND	Ground		**57**		GND	Ground	
28	CML-O	RX1n	Receiver Data Inverted		**58**	CML-I	TX1n	Transmitter Data Inverted	
29	CML-O	RX1p	Receiver Data Non-Inverted		**59**	CML-I	TX1p	Transmitter Data Non-Inverted	
30		GND	Ground		**60**		GND	Ground	

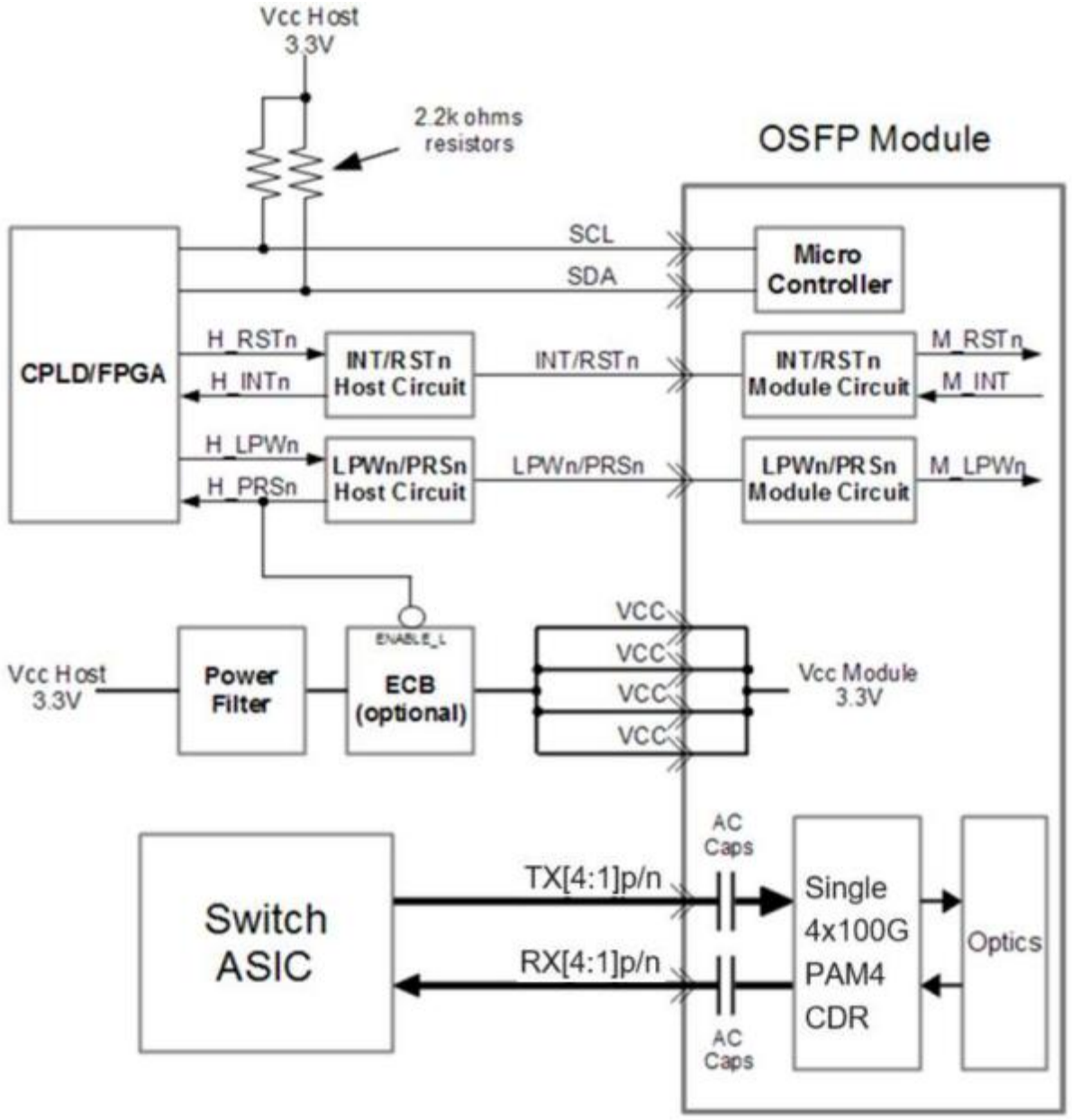
Note:

1. Not used

MECHANICAL DIMENSIONS (UNIT: mm)



RECOMMENDED HOST BOARD



Recommended OSFP Host Board Schematic

DIGITAL DIAGNOSTICS

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	ºC	Internal
Voltage	3.135 to 3.465	±3%	V	Internal
Tx Bias Current (Each Lane)	0 to 15	10%	mA	Internal
Tx Output Power (Each Lane)	-4.6 to +4	±3	dB	Internal
Rx Receive Power (Each Lane)	-6.3 to +4	±3	dB	Internal