

OSFP-400G-SR4-50-IB

400GBase OSFP SR4 InfiniBand Transceiver

Hot Pluggable, +3.3V, MPO-12, 850nm, MMF, 50m, Commercial Temperature

FEATURES

- Hot-pluggable OSFP form factor
- VCSEL transmitter and PIN PD receiver
- Support 425Gb/s aggregate bit rate
- Support both 4x100G Ethernet and InfiniBand NDR
- Compliant with IEEE 802.3-2022:
 - 4x100GBASE-VR1 optical interface
- Compliant with IEEE 802.3ck-2022:
 - 4x100GAUI-1 C2M electrical interface
- Compliant with InfiniBand Trade Association (IBTA) Specification 1.6
 - InfiniBand NDR electrical and optical interface
- Compliant with OSFP MSA Specification Rev 5.0 RHS housing (with the longer body:107.8mm) with MPO-12/APC receptacle
- Compliant with CMIS Rev 5.0
- Commercial Operating Temperature Range: 0°C to 70°C
- Power dissipation < 9W
- Two wire serial Interface with digital diagnostic monitoring
- Complies with EU Directive 2011/65/EU (RoHS compliant)
- Class 1 Laser

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T _s	-40	85	°C
Supply Voltage	V _{CC}	-0.5	3.6	V
Relative Humidity (non-condensing)	RH	5	85	%
Data Input Voltage Differential	V _{DIP} -V _{DIN}	-	1	V
Control Input Voltage	V _I	-0.3	VCC+0.5	V
Control Output Current	I _o	-20	20	mA

RECOMMENDED OPERATING ENVIRONMENT

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Operating Case Temperature	T _{OPR}	0	-	70	°C	
Power Supply Voltage	V _{CC}	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	I _{CC_IP}	-	-	3600	mA	
Sustained peak current at hot plug	I _{CC_SP}	-	-	2997	mA	
Maximum Power Dissipation	P _D	-	-	9	W	
Maximum Power Dissipation, Low Power Mode	P _{DLP}	-	-	2	W	
Signalling Speed per Lane	DRL	-	53.125	-	GBd	
Control Input Voltage High	V _{IH}	V _{CC} *0.7	-	V _{CC} +0.3	V	
Control Input Voltage Low	V _{IL}	-0.3	-	V _{CC} *0.3	V	
Two Wire Serial Interface Clock Rate	-	-	-	400	kHz	
Power Supply Noise 1 kHz - 1 MHz (p-p)	-	-	-	66	mVpp	
Operating Distance	-	2	-	50	m	1

Note:

- 0.5 m to 30 m for OM3, 0.5 m to 50 m for OM4 and OM5, with FEC.

OPTICAL PARAMETERS

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
TRANSMITTER						
Signaling rate, each lane (range)	-	53.125 ± 100 ppm			GBd	
Wavelength	λC	844	-	860	nm	
RMS spectral width	RMS	-	-	0.65	dB	1
Average Launch Power, each lane	AOPL	-4.6	-	4	dBm	
Outer Optical Modulation Amplitude (OMA _{outer}), each lane for max (TECQ, TDECQ) ≤ 1.8 dB for 1.8 < max (TECQ, TDECQ) ≤ 4.4 dB	OMA _{outer}	-2.6 -4.4+max(TECQ, TDECQ)	-	3.5	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	-	-	4.4	dB	
Transmitter eye closure for PAM4 (TECQ), each lane	TECQ	-	-	4.4	dB	
Over/under-shoot	-	-	-	29	%	
Transmitter power excursion, each lane	-	-	-	2.3	dBm	
Average Launch Power of OFF Transmitter, each lane	TOFF	-	-	-30	dBm	
Extinction Ratio, each lane	ER	2.5	-	-	dB	
Transmitter transition time, each lane	Tr	-	-	17	ps	
RIN _{14OMA}	RIN	-	-	-132	dB/Hz	
Optical return loss tolerance	ORL	-	-	14	dB	
Encircled flux	-	≥86% at 19μm ≤30% at 4.5μm				
RECEIVER						
Signaling rate, each lane (range)	-	53.125 ± 100 ppm			GBd	
Wavelength	λC	840	-	860	nm	
Damage Threshold, each Lane	AOPD	5	-	-	dBm	

Average Receive Power, each Lane	AOPR	-6.3	-	4	dBm	
Receive Power (OMAuter), each Lane	OMAR	-	-	3.5	dBm	
Receiver Reflectance	RR	-	-	-15	dB	
Receiver sensitivity (OMAuter) for TECQ < 1.4 dB for 1.4 dB ≤ TECQ ≤ 3.4 dB	SOMA	-	-	-4.4 -6.2 +TECQ	dBm	
Stressed Receiver Sensitivity (OMAuter), each Lane	SRS	-	-	-1.8	dBm	2
CONDITIONS OF STRESSED RECEIVER SENSITIVITY TEST						
Stressed eye closure for PAM4 (SECQ), lane under test	SECQ	-	4.4	-	dB	
OMAuter of each aggressor lane		-	3.5	-	dBm	

Note:

1. RMS spectral width is the standard deviation of the spectrum
2. Measured with conformance test signal at TP3 for the BER = 2.4×10^{-4}

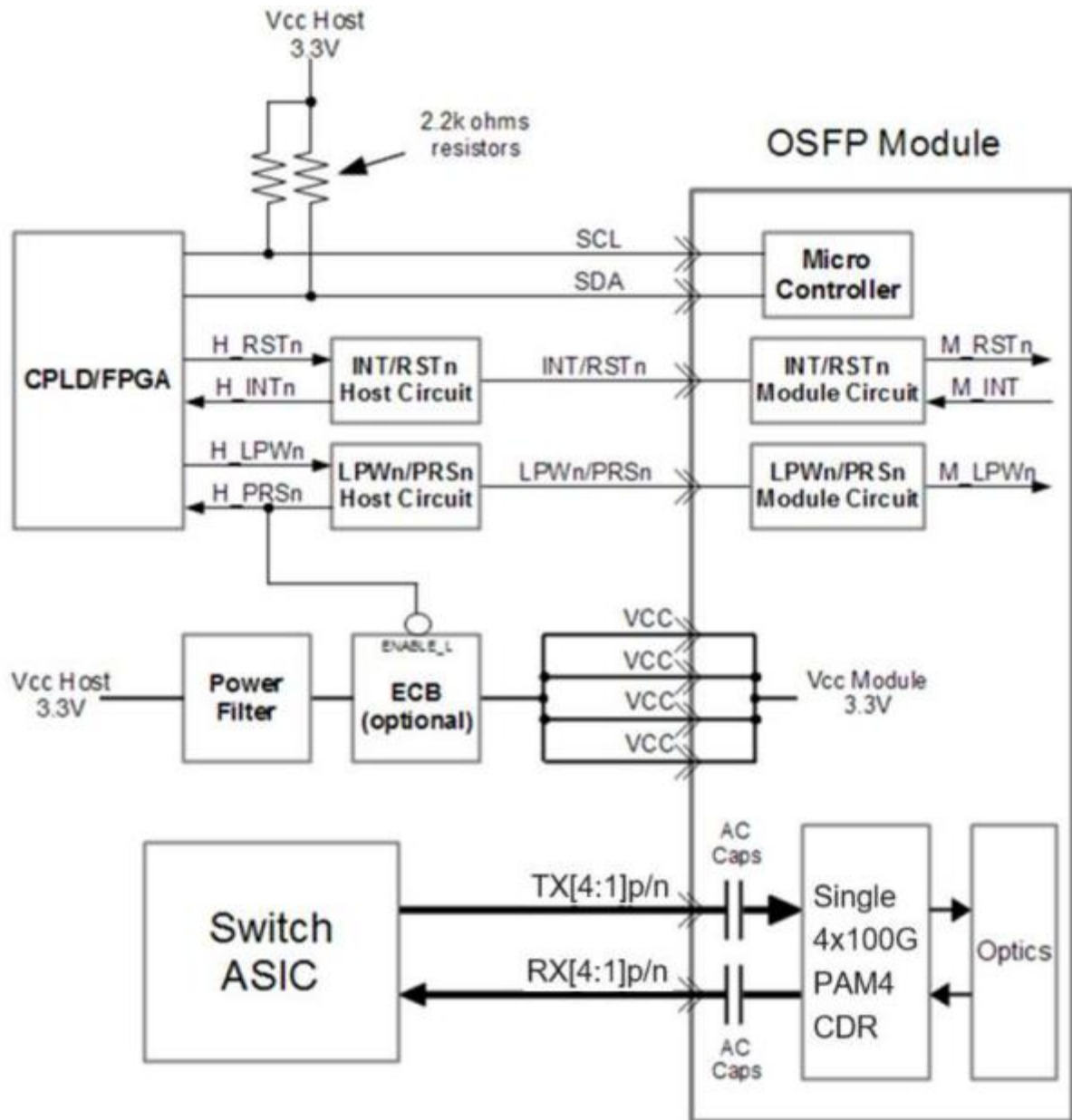
ELECTRICAL CHARACTERISTICS (HIGH SPEED SIGNAL)

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
TRANSMITTER (Module Input, TP1)						
Differential pk-pk input Voltage tolerance (TP1a)	-	750	-	-	mV	
Peak-to-peak AC common-mode voltage tolerance Low-frequency, VCMLF Full-band, VCMFB	-	32 80	-	-	mV	
Differential-mode to common-mode return loss	RLcd	802.3ck 120G-2			dB	
Effective return loss	ERL	8.5	-	-	dB	
Differential termination mismatch	-	-	-	10	%	
Single-ended voltage tolerance range	-	-0.4	-	3.3	V	
DC common-mode voltage tolerance	-	-0.35	-	2.85	V	
RECEIVER (Module Output, TP4)						
Peak-to-peak AC common-mode voltage Low-frequency, VCMLF Full-band, VCMFB	-	-	-	32 80	mV	
Differential peak-to-peak output voltage Short mode Long mode	-	-	-	600 845	mV	
Eye height	EH	15	-	-	mV	
Vertical eye closure	VEC	-	-	12	dB	
Common-mode to differential-mode return loss	RLDc	802.3ck 120G-1			dB	
Effective return loss	ERL	8.5	-	-	dB	
Differential termination mismatch	-	-	-	10	%	
Transition time	-	8.5	-	-	ps	
DC common-mode voltage tolerance	-	-0.35	-	2.85	V	

ELECTRICAL CHARACTERISTICS (LOW SPEED CONTROL & SENSE SIGNALS)

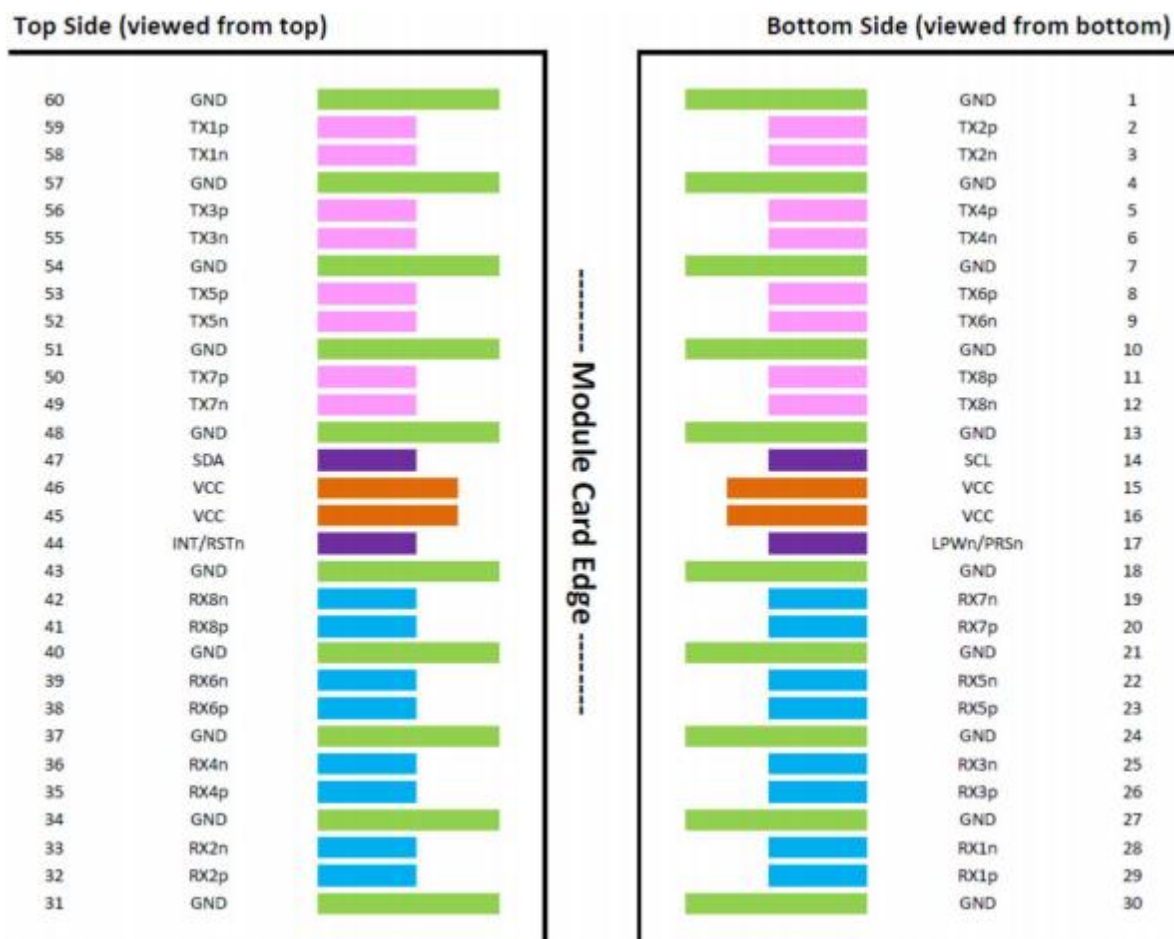
Parameter	Symbol	Min.	Max.	Unit
Module output SCL and SDA	VOL	0	0.4	V
Module Input SCL and SDA	VIL	-0.3	VCC*0.3	V
	VIH	VCC*0.7	VCC+0.5	V
INT/RSTn	Compliant with OSFP MSA 5.0 Table 13-4			

RECOMMENDED CIRCUIT



Recommended Host Board Schematic

PIN ASSIGNMENT



Pinout Definitions of OSFP Module Inputs/Outputs

Pin	Symbol	Description	Logic	Notes	Pin	Symbol	Description	Logic	Note
1	GND	Ground			31	GND	Ground		
2	TX2p	Transmitter Data Non-Inverted	CML-I		32	RX2p	Receiver Data Non-Inverted	CML-O	
3	TX2n	Transmitter Data Inverted	CML-I		33	RX2n	Receiver Data Inverted	CML-O	
4	GND	Ground			34	GND	Ground		
5	TX4p	Transmitter Data Non-Inverted	CML-I		35	RX4p	Receiver Data Non-Inverted	CML-O	
6	TX4n	Transmitter Data Inverted	CML-I		36	RX4n	Receiver Data Inverted	CML-O	
7	GND	Ground			37	GND	Ground		
8	TX6p	Transmitter Data Non-Inverted	CML-I	1	38	RX6p	Receiver Data Non-Inverted	CML-O	1
9	TX6n	Transmitter Data Inverted	CML-I	1	39	RX6n	Receiver Data Inverted	CML-O	1
10	GND	Ground			40	GND	Ground		
11	TX8p	Transmitter Data Non-Inverted	CML-I	1	41	RX8p	Receiver Data Non-Inverted	CML-O	1
12	TX8n	Transmitter Data Inverted	CML-I	1	42	RX8n	Receiver Data Inverted	CML-O	1
13	GND	Ground			43	GND	Ground		
14	SCL	2-wire Serial interface clock	LVCMS- I/O		44	INT/RS T n	Module Interrupt / Module Reset	Multi-Level	
15	VCC	+3.3V Power			45	VCC	+3.3V Power		
16	VCC	+3.3V Power			46	VCC	+3.3V Power		
17	LPWn/ P RSn	Low-Power Mode / Module Present	Multi-Level		47	SDA	2-wire Serial interface data	LVCMS- I/O	
18	GND	Ground			48	GND	Ground		
19	RX7n	Receiver Data Inverted	CML-O	1	49	TX7n	Transmitter Data Inverted	CML-I	1
20	RX7p	Receiver Data Non-Inverted	CML-O	1	50	TX7p	Transmitter Data Non-Inverted	CML-I	1
21	GND	Ground			51	GND	Ground		
22	RX5n	Receiver Data Inverted	CML-O	1	52	TX5n	Transmitter Data Inverted	CML-I	1
23	RX5p	Receiver Data Non-Inverted	CML-O	1	53	TX5p	Transmitter Data Non-Inverted	CML-I	1
24	GND	Ground			54	GND	Ground		
25	RX3n	Receiver Data Inverted	CML-O		55	TX3n	Transmitter Data Inverted	CML-I	
26	RX3p	Receiver Data Non-Inverted	CML-O		56	TX3p	Transmitter Data Non-Inverted	CML-I	
27	GND	Ground			57	GND	Ground		
28	RX1n	Receiver Data Inverted	CML-O		58	TX1n	Transmitter Data Inverted	CML-I	
29	RX1p	Receiver Data Non-Inverted	CML-O		59	TX1p	Transmitter Data Non-Inverted	CML-I	
30	GND	Ground			60	GND	Ground		

Module Pin Definitions

Note:

1. Not used

DIGITAL DIAGNOSTICS

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	°C	Internal
Voltage	3.135 to 3.465	±3%	V	Internal
Tx Bias Current (Each Lane)	0 to 15	10%	mA	Internal
Tx Output Power (Each Lane)	-4.6 to +4	±3	dB	Internal
Rx Receive Power (Each Lane)	-6.3 to +4	±3	dB	Internal

MECHANICAL DIMENSIONS (UNIT: mm)

