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Technical Datasheet

QSFP-DD-800G-SR8

800G QSFP-DD SR8 Transceiver

Hot Pluggable, +3.3V, MPO-16, 850nm, MMF, 50m, Commercial Temperature

FEATURES

- Hot-pluggable QSFP-DD form factor
- VCSEL transmitter and PIN PD receiver
- Support 850Gb/s aggregate bit rate
- Compliant with IEEE 802.3-2022: 8x100GBASE-SR1 optical interface
- Compliant with IEEE 802.3ck-2022: 8x100GAUI-1 C2M electrical interface
- Compliant with QSFP-DD HW Specification Rev 6.3 type 2A housing with MPO-16
- Compliant with CMIS Rev 5.0
- Two wire serial Interface with digital diagnostic monitoring
- Complies with EU Directive 2011/65/EU (RoHS compliant)
- Class 1 Laser
- Commercial Operating Temperature Range: 0 to 70°C

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	TS	-40	85	ºC
Supply Voltage	VCC	-	3.6	V
Relative Humidity (non-condensing)	RH	5	85	%
Data Input Voltage Differential	$\|V_{DIP}-V_{DIN}\|$	-	1	V
Control Input Voltage	VI	-0.3	VCC+0.3	V
Control Output Current	IO	-20	20	mA

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RECOMMENDED OPERATING ENVIRONMENT

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Operating Case Temperature	T_{OPR}	0	-	70	ºC	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	I_{CC_IP}	-	-	TBD	mA	
Sustained peak current at hot plug	I_{CC_SP}	-	-	TBD	mA	
Maximum Power Dissipation	P_D	-	-	TBD	W	
Maximum Power Dissipation, Low Power Mode	P_{DLP}	-	-	1.5	W	
Signalling Speed per Lane	DRL	-	53.125	-	GBd	
Control Input Voltage High	V_{IH}	VCC*0.7	-	VCC+0.3	V	
Control Input Voltage Low	V_{IL}	-0.3	-	VCC*0.3	V	
Two Wire Serial Interface Clock Rate	-	-	-	400	kHz	
Power Supply Noise 1 kHz - 1 MHz (p-p)	-	-	-	66	mVpp	
Operating Distance	-	2	-	50	m	1

Notes:

1. 0.5 m to 30 m for OM3, 0.5 m to 50 m for OM4 and OM5, with FEC.

OPTICAL PARAMETERS

Parameter	Symbol	Min	Typical	Max	Unit	Notes
TRANSMITTER						
Signalling rate, each lane (range)	-	53.125 ± 100 ppm			GBd	
Wavelength	λ_C	840	850	860	nm	
RMS spectral width	RMS	-	-	0.6	dB	1
Average Launch Power, each lane	AOP_L	-4.6	-	4	dBm	
Outer Optical Modulation Amplitude (OMAouter), each lane for max (TECQ, TDECQ) <= 1.8 dB for 1.8 < max (TECQ, TDECQ) <= 4.4 dB	OMAouter	-2.6-4.4+max (TECQ, TDECQ)	-	3.5	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	-	-	TBD	dB	
Transmitter eye closure for PAM4 (TECQ), each lane	TECQ	-	-	TBD	dB	
Over/under-shoot	-	-		29	%	
Transmitter power excursion, each lane	-	-		2.3	dBm	
Average Launch Power of OFF Transmitter, each lane	T_{OFF}	-	-	-30	dBm	
Extinction Ratio, each lane	ER	2.5	-	-	dB	
Transmitter transition time, each lane	Tr	-	-	17	ps	
$RIN_{14}OMA$	RIN			-132	dB/Hz	
Optical return loss tolerance	ORL			14	dB	
Encircled flux		>=86% at 19μm <=30% at 4.5μm				
RECEIVER						
Signalling rate, each lane (range)	-	53.125 ± 100 ppm			GBd	
Wavelength	λ_C	840	850	860	nm	
Damage Threshold, each Lane	AOP_D	5	-	-	dBm	
Average Receive Power, each Lane	AOP_R	-6.4	-	4	dBm	
Receive Power (OMAouter), each Lane	OMA_R	-	-	3.5	dBm	
Receiver Reflectance	RR	-	-	-15	dB	
Receiver sensitivity (OMAouter) for TECQ < 1.4 dB for 1.4 dB <=TECQ<=3.4 dB	S_{OMA}	-	-	-4.6 -6.4 + TECQ	dBm	
Stressed Receiver Sensitivity (OMAouter), each Lane	SRS	-	-	-2	dBm	2
CONDITIONS OF STRESSED RECEIVER SENSITIVITY TEST						
Stressed eye closure for PAM4 (SECQ), lane under test	SECQ	-	4.4	-	dB	
OMAouter of each aggressor lane			3.5		dBm	

Note:

1. RMS spectral width is the standard deviation of the spectrum
2. Measured with conformance test signal at TP3 for the BER = 2.4x10-4

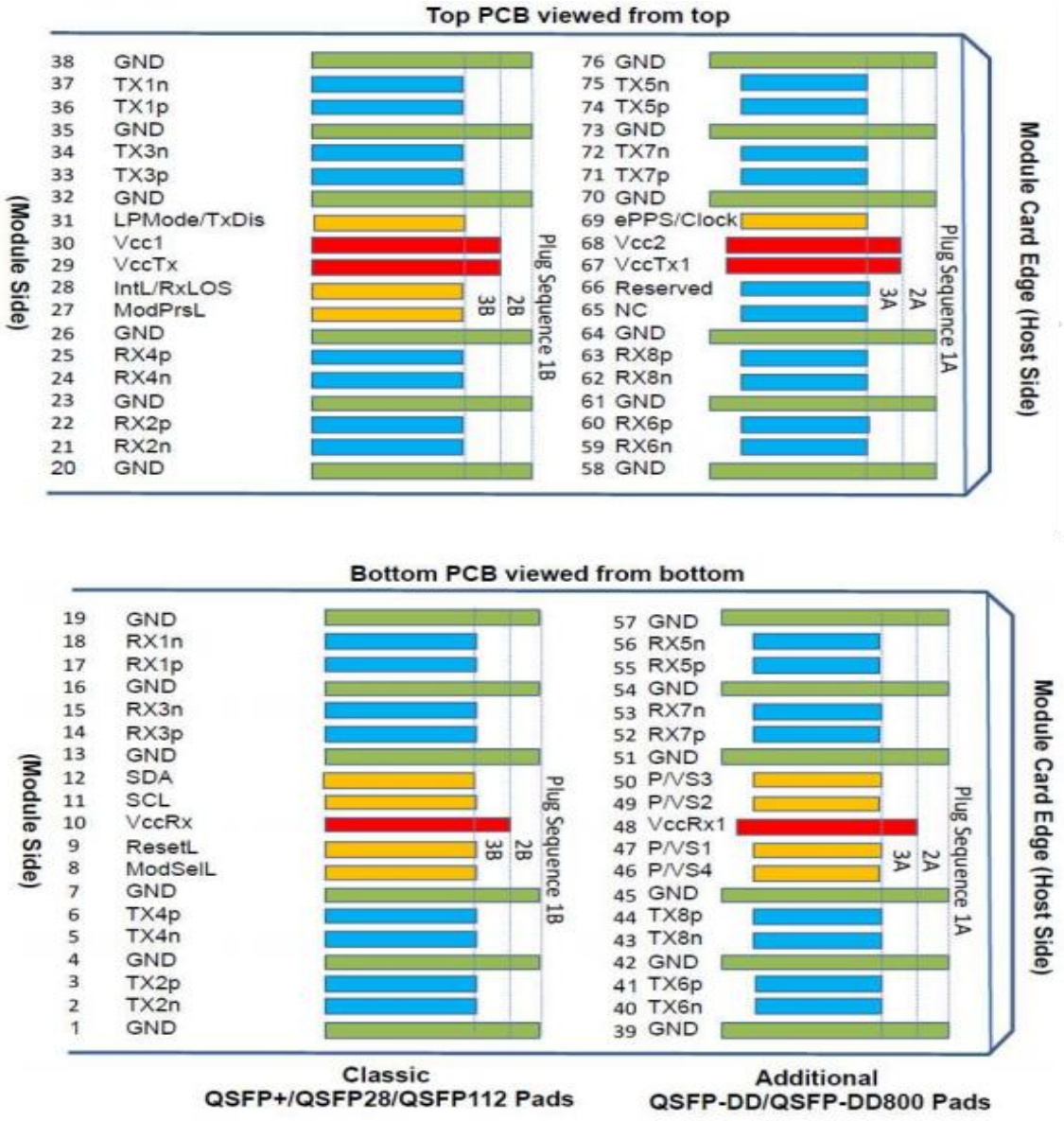
ELECTRICAL CHARACTERISTICS (High Speed Signal - compliant with IEEE802.3ck C2M)

Parameter	Symbol	Min	Typical	Max	Unit	Note
TRANSMITTER						
Differential pk-pk input Voltage tolerance (TP1a)	-	750	-	-	mV	
Peak-to-peak AC common-mode voltage tolerance {Low-frequency, VCMLF; Full-band, VCMFB}	-	{32; 80}	-	-	mV	
Differential-mode to common-mode return loss	RLcd	802.3ck 120G-2			dB	
Effective return loss	ERL	8.5	-	-	dB	
Differential termination mismatch	-	-	-	10	%	
Single-ended voltage tolerance range	-	-0.4	-	3.3	V	
DC common-mode voltage tolerance	-	-0.35	-	2.85	V	
RECEIVER						
Peak-to-peak AC common-mode voltage {Low-frequency, VCMLF; Full-band, VCMFB}	-	-	-	{32; 80}	mV	
Differential peak-to-peak output voltage {Short mode; Long mode}	-	-	-	{600; 845}	mV	
Eye height	EH	15	-	-	mV	
Vertical eye closure	VEC	-	-	12	dB	
Common-mode to differential-mode return loss	RLDc	802.3ck 120G-1			dB	
Effective return loss	ERL	8.5	-	-	dB	
Differential termination mismatch	-	-	-	10	%	
Transition time	-	8.5	-	-	ps	
DC common-mode voltage tolerance	-	-0.35	-	2.85	V	

ELECTRICAL CHARACTERISTICS (Low Speed Control and Sense Signals - compliant with QSFP-DD HW Rev 6.3 Table 16)

Parameter	Symbol	Min.	Max.	Unit
Module output SCL and SDA	VOL	0	0.4	V
Module Input SCL and SDA	VIL	-0.3	VCC*0.3	V
	VIH	VCC*0.7	VCC+0.5	V
InitMode, ResetL and ModSelL	VIL	-0.3	0.8	V
	VIH	2	VCC+0.3	V
IntL	VOL	0	0.4	V
	VOH	VCC-0.5	VCC+0.3	V

PIN ASSIGNMENT



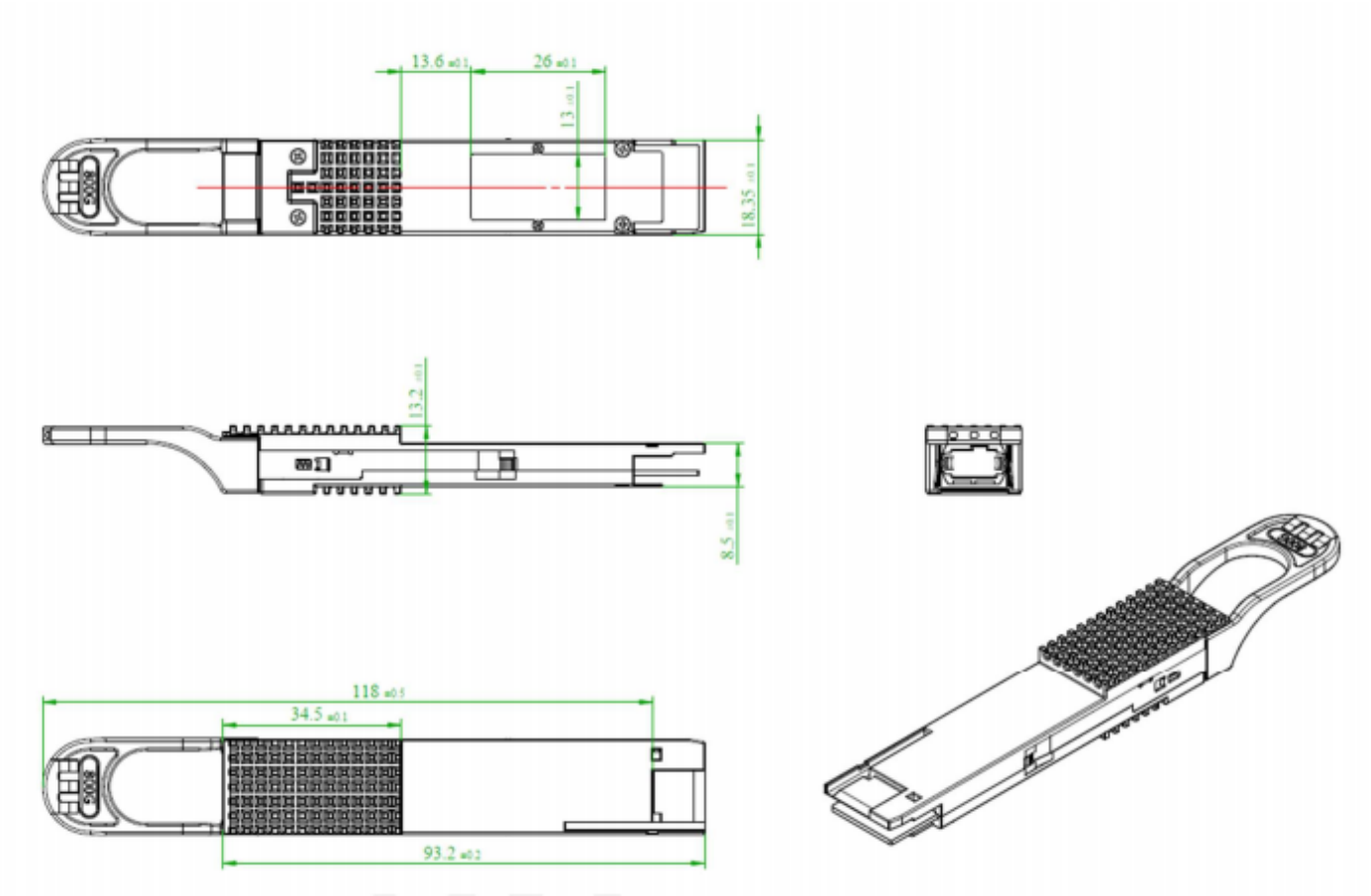
Pin definitions of the module high speed inputs/outputs

Pin	Logic	Symbol	Description	Pin	Logic	Symbol	Description
1		GND	Ground	**39**		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	**40**	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	**41**	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	**42**		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	**43**	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	**44**	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	**45**		GND	Ground
8	LVTTL-I	ModSelL	Module Select	**46**	LVCMOS /CML-I	P/VS4	Programmable/Module Vendor Specific 4
9	LVTTL-I	ResetL	Module Reset	**47**	LVCMOS /CML-I	P/VS1	Programmable/Module Vendor Specific 1
10		VccRx	+3.3V Power Supply Receiver	**48**		VccRx1	3.3V Power Supply
11	LVCMOS -I/O	SCL	TWI serial interface clock	**49**	LVCMOS /CML-O	P/VS2	Programmable/Module Vendor Specific 2
12	LVCMOS -I/O	SDA	TWI serial interface data	**50**	LVCMOS /CML-O	P/VS3	Programmable/Module Vendor Specific 3
13		GND	Ground	**51**		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	**52**	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	**53**	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	**54**		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	**55**	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	**56**	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	**57**		GND	Ground
20		GND	Ground	**58**		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	**59**	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	**60**	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	**61**		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output	**62**	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	**63**	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	**64**		GND	Ground
27	LVTTL-O	ModPrsL	Module Present	**65**		NC	Not connected
28	LVTTL-O	IntL/Rx LOS	Interrupt/optional RxLOS	**66**		Reserved	

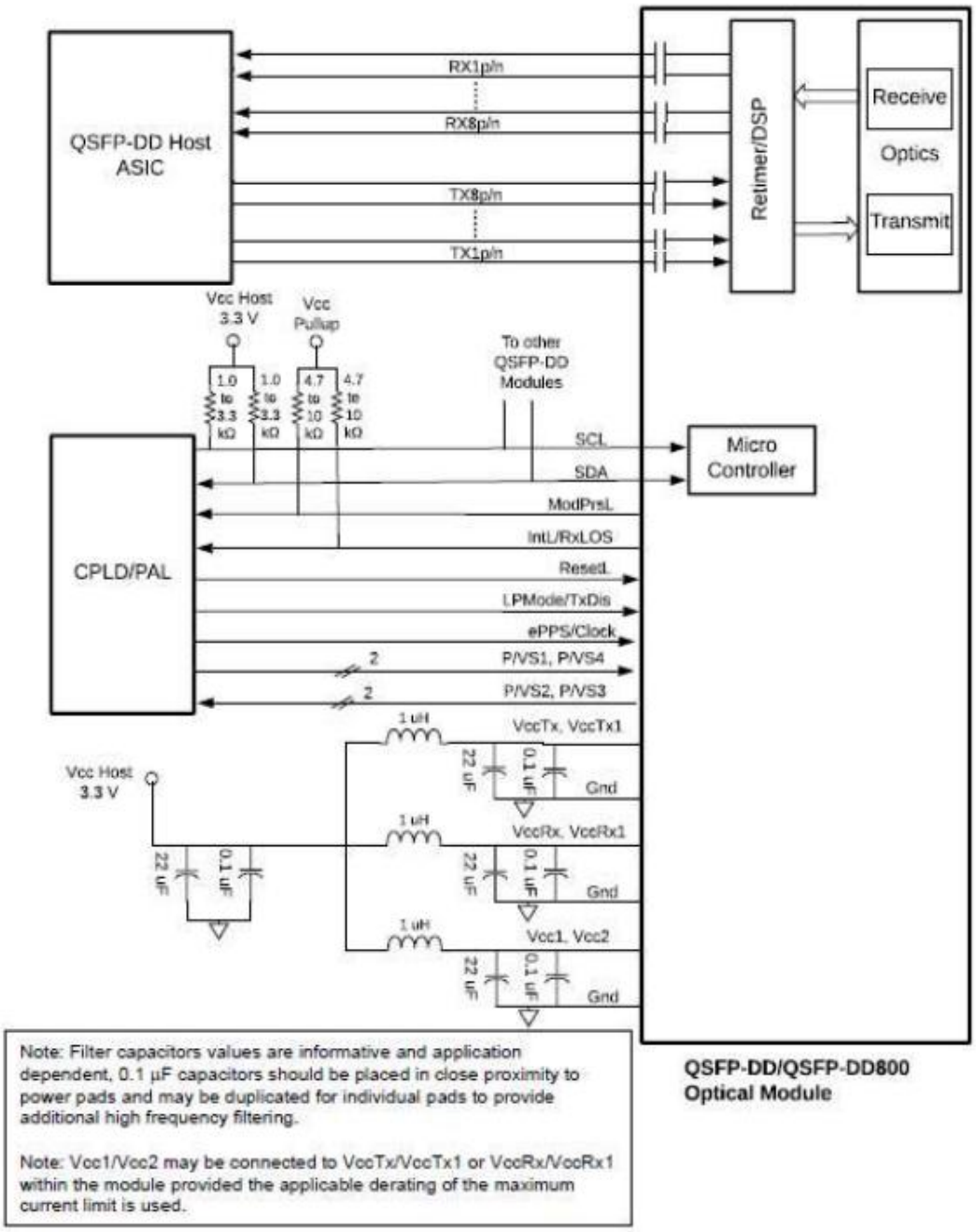
CONTINUED:

29		VccTx	+3.3V Power Supply Transmitter	**67**		VccTx1	3.3V Power Supply
30		Vcc1	+3.3V Power Supply	**68**		Vcc2	3.3V Power Supply
31	LVTTL-I	LPMode/TxDis	Low Power mode/optional TX Disable	**69**	LVCMO S-I	ePPS/ Clock	1PPS PTP clock or reference clock input
32		GND	Ground	**70**		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	**71**	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	**72**	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	**73**		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	**74**	CML-I	Tx5p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input	**75**	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	**76**		GND	Ground

MECHANICAL DIMENSIONS (UNIT: mm)



RECOMMENDED HOST BOARD



Recommended QSFP-DD/QSFP-DD800 Host Board Schematic

DIGITAL DIAGNOSTICS

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	ºC	Internal
Voltage	0 to VCC	0.1	V	Internal
Tx Bias Current (Each Lane)	0 to 15	10%	mA	Internal
Tx Output Power (Each Lane)	-4.6 to +4	±3	dB	Internal
Rx Receive Power (Each Lane)	-6.4 to +4	±3	dB	Internal