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Technical Datasheet

QSFP-DD-800G-DR8

800G QSFP-DD DR8 Transceiver

Hot Pluggable, +3.3V, MPO-16, 1310nm, MMF, 500m, Commercial Temperature

FEATURES

- Compliant with IEEE 802.3cu-2021: 8x100GBASE-DR optical interface
- Compliant with IEEE P802.3ck D3.0: 8x100GAUI-1 C2M electrical interface
- Compliant with QSFP-DD MSA HW Rev 6.01 type 2A with MPO-16 connector
- Compliant with CMIS Rev 5.0
- Two wire serial Interface with digital diagnostic monitoring
- Complies with EU Directive 2011/65/EU (RoHS compliant)
- Class 1 Laser
- Commercial operating temperature range: 0 to 70°C

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	85	ºC
Supply Voltage	V_{CC}	-0.5	3.6	V
Relative Humidity (non-condensing)	RH	5	95	%
Data Input Voltage Differential	$\lvert V_{DIP}-V_{DIN}\rvert$	-	1	V
Control Input Voltage	V_I	-0.3	V_{CC}+0.5	V
Control Output Current	I_O	-20	20	mA

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RECOMMENDED OPERATING ENVIRONMENT

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Operating Case Temperature	T_{OPR}	0	-	70	ºC	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	I_{CC_IP}	-	-	TBD	mA	
Sustained peak current at hot plug	I_{CC_SP}	-	-	TBD	mA	
Maximum Power Dissipation	P_D	-	-	TBD	W	
Maximum Power Dissipation, Low Power Mode	P_{DLP}	-	-	TBD	W	
Signalling Speed per Lane	DRL	-	53.125	-	GBd	
Control Input Voltage High	V_{IH}	V_{CC}*0.7	-	V_{CC}+0.3	V	
Control Input Voltage Low	V_{IL}	-0.3	-	V_{CC}*0.3	V	
Two Wire Serial Interface Clock Rate	-	-	-	400	kHz	
Power Supply Noise 1 kHz - 1 MHz (p-p)	-	-	-	66	mVpp	
Operating Distance	-	2	-	500	m	

OPTICAL PARAMETERS

Parameter	Symbol	Min	Typical	Max	Unit	Notes
TRANSMITTER						
Wavelength	λ_C	1304.5	1311	1317.5	nm	
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Average Launch Power, each lane	AOP_L	-2.9	-	4.0	dBm	1
Outer Optical Modulation Amplitude (OMAouter), each Lane	T_{OMA}	-0.8	-	4.2	dBm	
Launch power in OMAouter minus TDECQ, each lane: **for extinction ratio >= 5 dB** **for extinction ratio < 5 dB**	$T_{OMA-TDECQ}$	 -2.2 -1.9	-	-	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	-	-	3.4	dB	
TDECQ – 10log10(Ceq), each lane	Ceq	-	-	3.4	dB	
Average Launch Power of OFF Transmitter, each lane	T_{OFF}	-	-	-15	dBm	
Extinction Ratio	ER	3.5	-	-	dB	
Transmitter transition time	Tr			17	ps	
$RIN_{15.5}OMA$	RIN	-	-	-136	dB/Hz	
Optical return loss tolerance	ORL	-	-	15.5	dB	
Transmitter Reflectance	T_R	-	-	-26	dB	2
RECEIVER						
Wavelength	λ_C	1304.5	1311	1317.5	nm	
Damage Threshold, each Lane	AOP_D	5	-	-	dBm	
Average Receive Power, each Lane	AOP_R	-5.9	-	4	dBm	
Receive Power (OMAouter), each Lane	OMA_R	-	-	4.2	dBm	
Receiver Reflectance	RR	-	-	-26	dB	
Receiver Sensitivity (OMAouter), each Lane	S_{OMA}	-	-	Max (–3.9, SECQ – 5.3)	dBm	3
Stressed Receiver Sensitivity (OMAouter), each Lane	SRS	-	-	-1.9	dBm	4
Conditions of stressed receiver sensitivity test						
Stressed eye closure for PAM4 (SECQ), lane under test	SECQ	-	3.4	-	dB	
SECQ – 10log10(Ceq), lane under test	Ceq	-	-	3.4	dB	
OMAouter of each aggressor lane		-	4.2	-	dBm	

Note:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength
2. Transmitter reflectance is defined looking into the transmitter.
3. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB.
4. Measured with conformance test signal at TP3 for the BER = 2.4x10-4

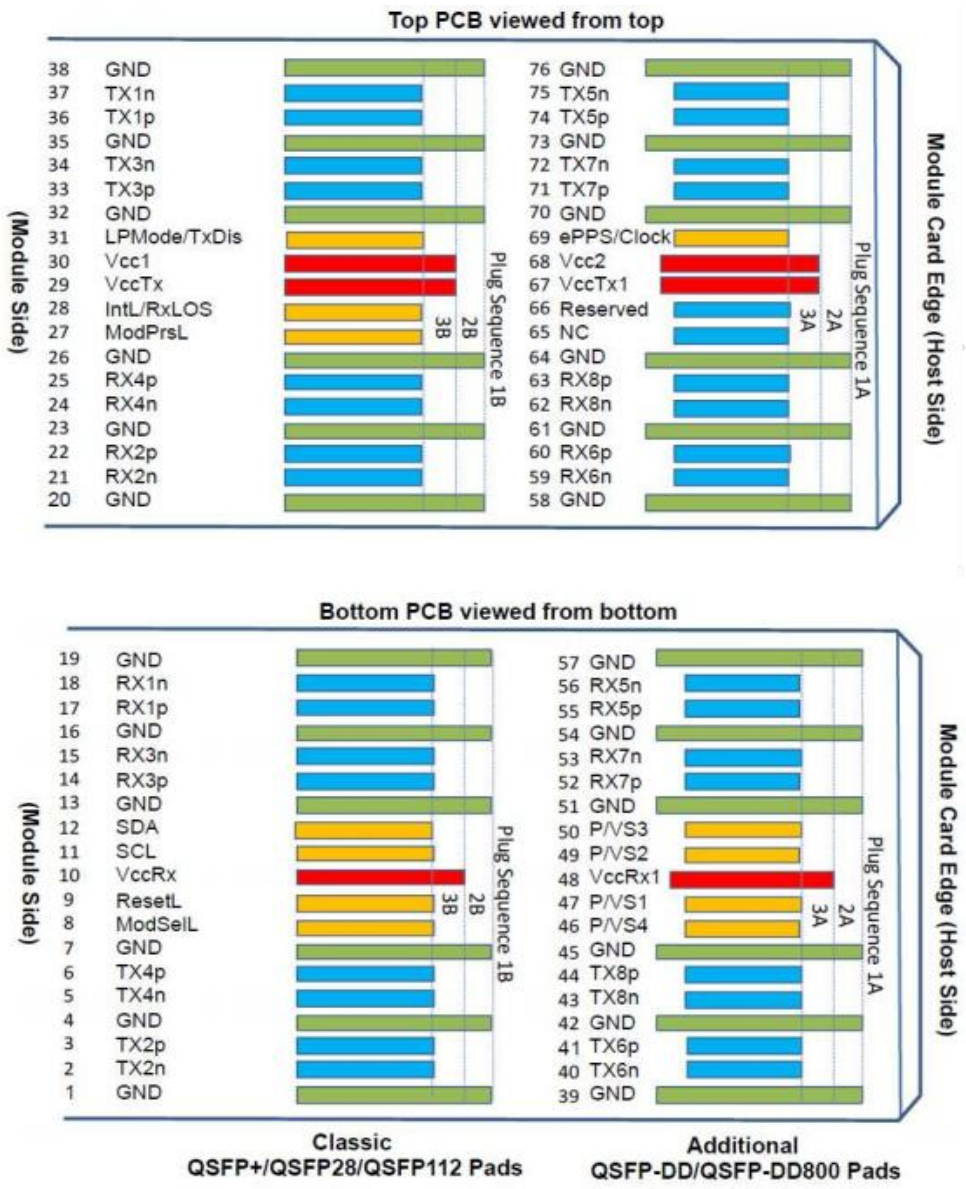
ELECTRICAL CHARACTERISTICS (High Speed Signal - compliant with IEEE802.3ck C2M)

Parameter	Symbol	Min	Typical	Max	Unit	Note
TRANSMITTER						
Differential pk-pk input Voltage tolerance (TP1a)	-	750	-	-	mV	
AC common-mode RMS voltage tolerance (TP1a)	-	25	-	-	mV	
Differential-mode to common-mode return loss	RLcd	802.3ck 120G-2			dB	
Effective return loss	ERL	8.5	-	-	dB	
Differential termination mismatch	-	-	-	10	%	
Single-ended voltage tolerance range	-	-0.4	-	3.3	V	
DC common-mode voltage tolerance	-	-0.35	-	2.85	V	
RECEIVER						
AC common-mode output Voltage (RMS)	-	-	-	25	mV	
Differential peak-to-peak output voltage {Short mode; Long mode}	-	-	-	{600; 845}	mV	
Eye height	EH	15	-	-	mV	
Vertical eye closure	VEC	-	-	12	dB	
Common-mode to differential-mode return loss	RLDc	802.3ck 120G-1			dB	
Effective return loss	ERL	8.5	-	-	dB	
Differential termination mismatch	-	-	-	10	%	
Transition time	-	8.5	-	-	ps	
DC common-mode voltage tolerance	-	-0.35	-	2.85	V	

ELECTRICAL CHARACTERISTICS (Low Speed Control and Sense Signals - compliant with QSFP-DD HW Rev6.01 Table 14)

Parameter	Symbol	Min.	Max.	Unit
Module output SCL and SDA	V_{OL}	0	0.4	V
Module Input SCL and SDA	V_{IL}	-0.3	V_{CC}*0.3	V
	V_{IH}	V_{CC}*0.7	V_{CC}+0.5	V
InitMode, ResetL and ModSelL	V_{IL}	-0.3	0.8	V
	V_{IH}	2	V_{CC}+0.3	V
IntL	V_{OL}	0	0.4	V
	V_{OH}	V_{CC}-0.5	V_{CC}+0.3	V

PIN ASSIGNMENT



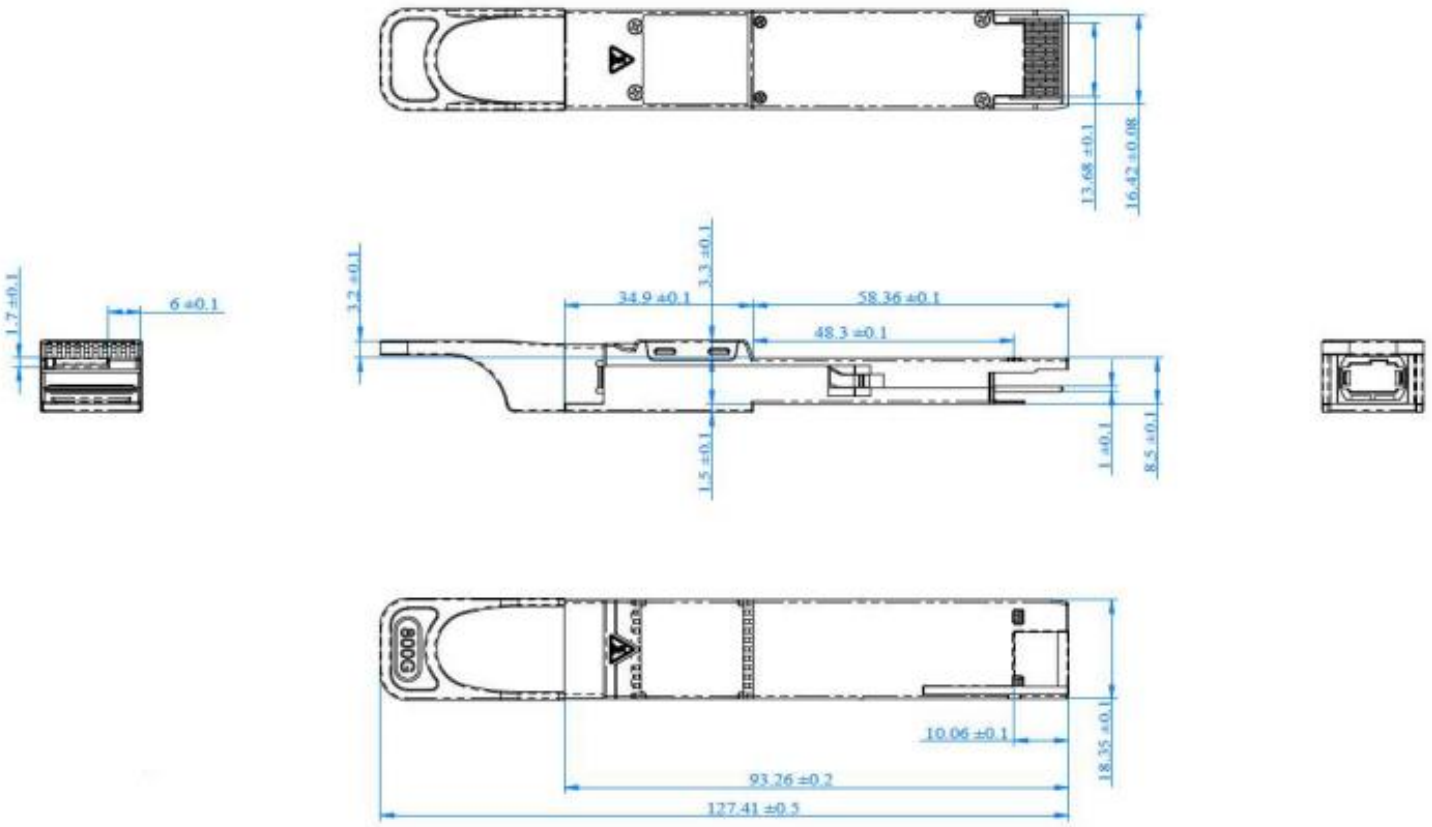
Pin definitions of the module high speed inputs/outputs

Pin	Logic	Symbol	Description	Pin	Logic	Symbol	Description
1		GND	Ground	**39**		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	**40**	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	**41**	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	**42**		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	**43**	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	**44**	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	**45**		GND	Ground
8	LVTTL-I	ModSelL	Module Select	**46**	LVCMOS/CML- I	P/VS4	Programmable/Module Vendor Specific 4
9	LVTTL-I	ResetL	Module Reset	**47**	LVCMOS /CML-I	P/VS1	Programmable/Module Vendor Specific 1
10		VccRx	+3.3V Power Supply Receiver	**48**		VccRx1	3.3V Power Supply
11	LVCMOS -I/O	SCL	TWI serial interface clock	**49**	LVCMOS /CML-O	P/VS2	Programmable/Module Vendor Specific 2
12	LVCMOS -I/O	SDA	TWI serial interface data	**50**	LVCMOS /CML-O	P/VS3	Programmable/Module Vendor Specific 3
13		GND	Ground	**51**		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	**52**	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	**53**	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	**54**		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	**55**	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	**56**	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	**57**		GND	Ground
20		GND	Ground	**58**		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	**59**	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	**60**	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	**61**		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output	**62**	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	**63**	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	**64**		GND	Ground
27	LVTTL-O	ModPrsL	Module Present	**65**		NC	Not connected
28	LVTTL-O	IntL/ RxLOS	Interrupt/optional RxLOS	**66**		Reserved	

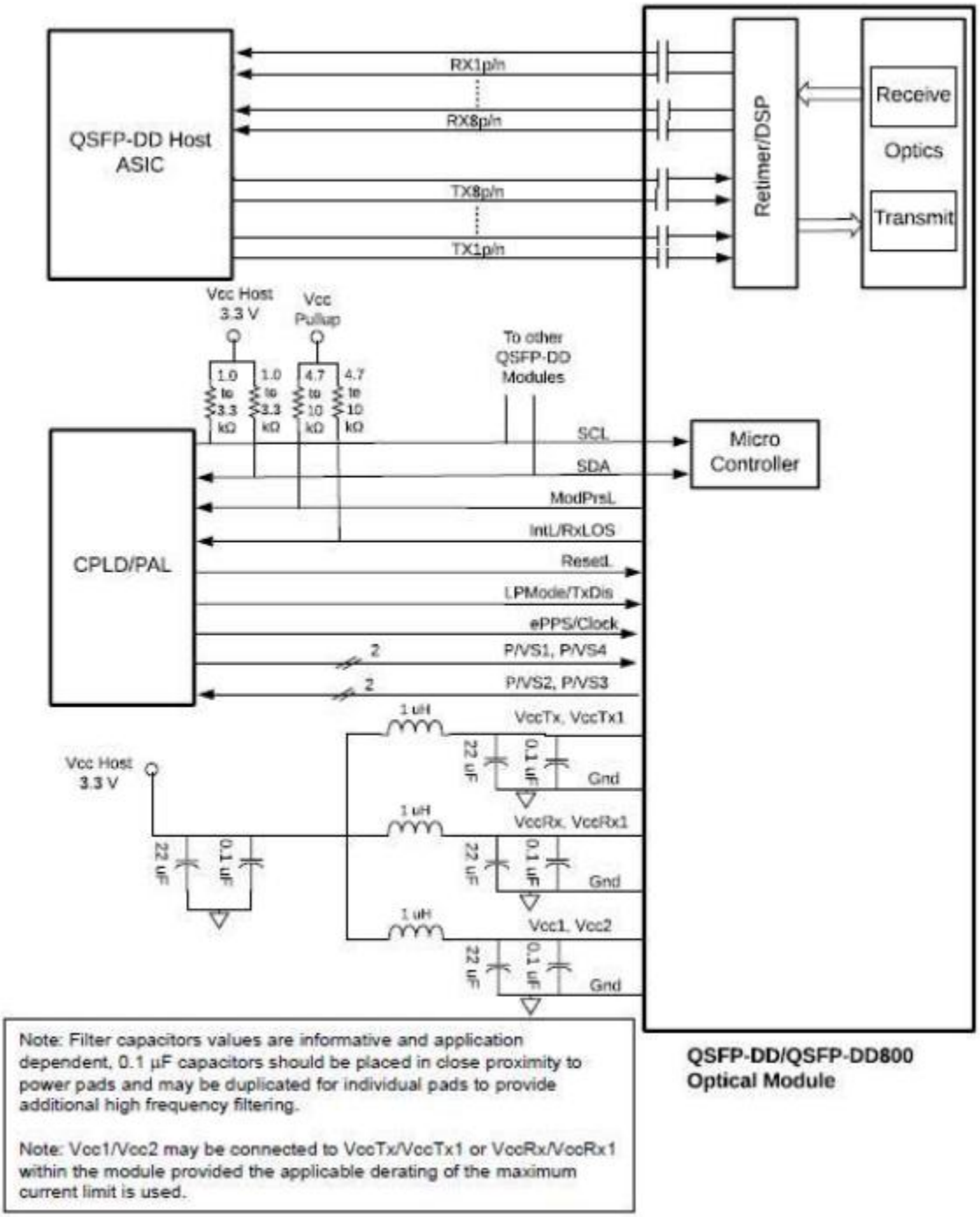
CONTINUED:

29		VccTx	+3.3V Power Supply Transmitter	**67**		VccTx1	3.3V Power Supply
30		Vcc1	+3.3V Power Supply	**68**		Vcc2	3.3V Power Supply
31	LVTTL-I	LPMode/TxDis	Low Power mode/optional TX Disable	**69**	LVCMO S-I	ePPS/ Clock	1PPS PTP clock or reference clock input
32		GND	Ground	**70**		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	**71**	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	**72**	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	**73**		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	**74**	CML-I	Tx5p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input	**75**	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	**76**		GND	Ground

MECHANICAL DIMENSIONS (UNIT: mm)



RECOMMENDED HOST BOARD



Recommended QSFP-DD/QSFP-DD800 Host Board Schematic

DIGITAL DIAGNOSTICS

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	ºC	Internal
Voltage	0 to Vcc	0.1	V	Internal
Tx Bias Current (Each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (Each Lane)	-2.9 to +4	±3	dB	Internal
Rx Receive Power (Each Lane)	-5.9 to +4	±3	dB	Internal