

QSFP-DD-400G-DR4-2

400GBase-DR4 QSFP-DD Transceiver

Hot Pluggable, +3.3V, MPO-12, 1310nm, SMF, 2km, Commercial Temperature

FEATURES

- Compliant with IEEE802.3bs standard: 400GAUI-8 electrical interface
- Compliant with IEEE 802.3cu standards: 4x100GBASE-LR1 optical interface
- Compliant with QSFP-DD MSA HW Rev 5.1
- Type 2 housing with MPO-12 connector
- Compliant with QSFP-DD CMIS Rev 4.0
- Maximum power consumption 10W
- Two wire serial Interface with digital diagnostic monitoring
- Complies with EU Directive 2011/65/EU (RoHS compliant)
- Class 1 Laser
- Commercial Operating Temperature Range: 0 to 70°C

APPLICATIONS

- 400GBASE-DR4 Ethernet
- Telecom Networking
- Data Centre Interconnect

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Storage Temperature	T _s	-40		85	°C	
Supply Voltage	V _{CC}	-0.5		3.6	V	
Relative Humidity (non-condensing)	RH	5		95	%	
Control Input Voltage	V _I	-0.3		V _{CC} +0.5	V	

RECOMMENDED OPERATING ENVIRONMENT

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T_{OPR}	0	-	70	°C	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	I_{CC_IP}	-	-	4000	mA	
Sustained peak current at hot plug	I_{CC_SP}	-	-	3300	mA	
Maximum Power Dissipation	P_D	-	-	10	W	
Maximum Power Dissipation, Low Power Mode	P_{DLP}	-	-	1.5	W	
Signalling Rate per Lane	SRL	-	53.125	-	GBd	PAM4
Two Wire Serial Interface Clock Rate	-	-	-	400	kHz	
Power Supply Noise Tolerance (10Hz - 10MHz)	-	-	-	66	mV	
Rx Differential Data Output Load	-	-	100	-	Ohm	
Operating Distance	-	2	-	2000	m	

OPTICAL PARAMETERS

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
TRANSMITTER						
Wavelength	λ_C	1304.5	1311	1317.5	nm	
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Average Launch Power, each lane	AOP_L	-1.9	-	4.8	dBm	1
Outer Optical Modulation Amplitude (OMA _{outer}), each lane	T_{OMA}	-	-	5	dBm	
Outer Optical Modulation Amplitude (OMA _{outer}), each lane: for TDECQ <1.4dB for 1.4 ≤ TDECQ ≤ 3.4dB	T_{OMA}	1.1 -0.3+TDECQ	-	-	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	-	-	3.4	dB	
Transmitter eye closure for PAM4(TECQ)	TECQ	-	-	3.4	dB	
TDECQ - TECQ	-	-	-	2.5	dB	
Over/under-shoot	-	-	-	22	%	
Transmitter power excursion	-	-	-	2.8	dBm	
Average Launch Power of OFF Transmitter, each lane	T_{OFF}	-	-	-15	dBm	
Extinction Ratio, each lane	ER	3.5	-	-	dB	
RIN _{15.6} OMA	RIN	-	-	-136	dB/Hz	
Optical Return Loss Tolerance	ORL	-	-	15.6	dB	
Transmitter Reflectance	T_R	-	-	-26	dB	
Transmitter Transition Time	T_t	-	-	17	ps	
RECEIVER						
Wavelength	λ_C	1304.5	1311	1317.5	nm	
Damage Threshold, each lane	AOP_D	5.8	-	-	dBm	
Average Receive Power, each lane	AOP_R	-8.2	-	4.8	dBm	2

CONTINUED

Receive Power (OMA _{outer}), each lane	OMA _R	-	-	5	dBm	
Receiver Reflectance	RR	-	-	-26	dB	
Receiver Sensitivity (OMA _{outer}), each lane for TECQ <1.4dB for 1.4 ≤ TECQ ≤ 3.4dB	S _{OMA}	-	-	-6.1 -7.5+TECQ	dBm	
Stressed Receiver Sensitivity (OMA _{outer}), each lane	SRS	-	-	-4.1	dBm	3
CONDITIONS OF STRESSED RECEIVER SENSITIVITY TEST						
Stressed eye closure for PAM4 (SECQ)			3.4		dB	

Note:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength.
2. Average receive power, (min) is informative and not the principal indicator of signal strength.
3. Measured with conformance test signal at TP3 for the BER = 2.4×10^{-4}

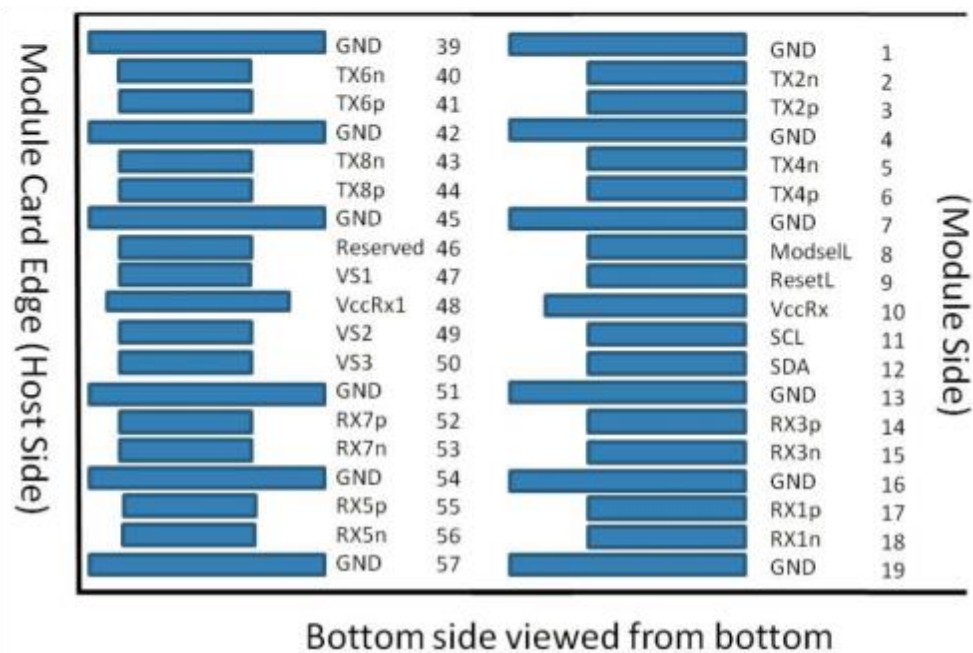
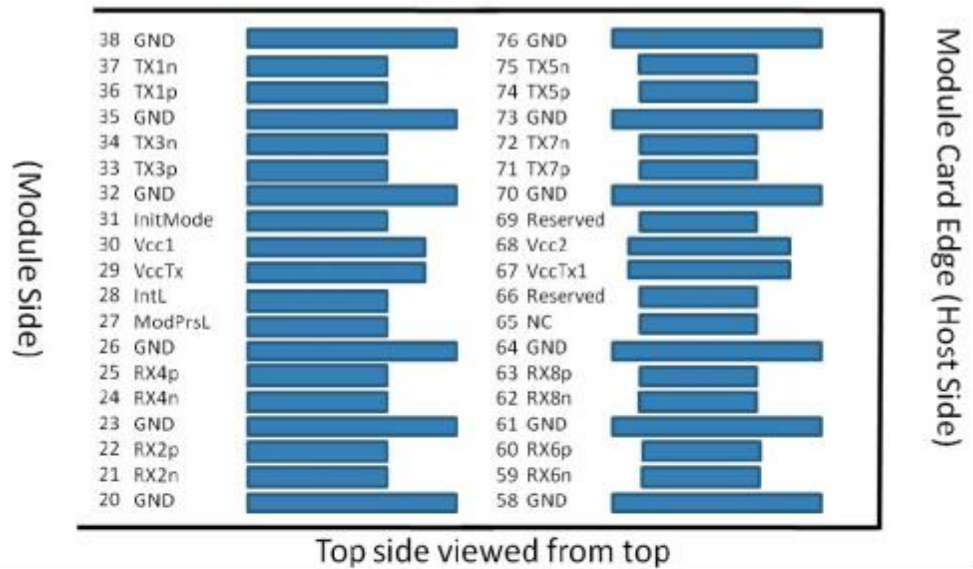
ELECTRICAL CHARACTERISTICS (High Speed Signal - Compliant with IEEE 802.3bs 400GAUI-8)

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
TRANSMITTER (Module Input)						
Differential pk-pk input Voltage tolerance		900	-	-	mV	
Differential termination mismatch		-	-	10	%	
Single-ended voltage tolerance range		-0.4	-	3.3	V	
DC common mode Voltage		-350	-	2850	mV	
RECEIVER (Module Output)						
AC common-mode output Voltage (RMS)		-	-	17.5	mV	
Differential output Voltage		-	-	900	mV	
Near-end Eye height, differential		70	-	-	mV	
Far-end Eye height, differential		30	-	-	mV	
Far end pre-cursor ISI ratio		-4.5	-	2.5	%	
Differential Termination Mismatch		-	-	10	%	
Transition Time (min, 20% to 80%)		9.5	-	-	ps	
DC common mode Voltage		-350	-	2850	mV	

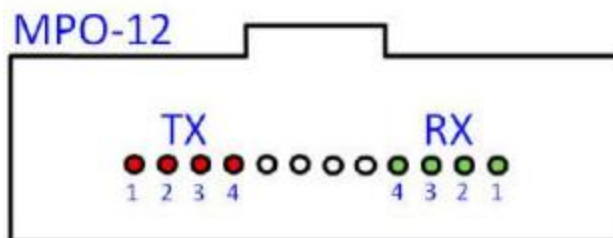
ELECTRICAL CHARACTERISTICS (Low Speed Signal - Compliant with QSFP-DD HW Rev 5.1)

Parameter	Symbol	Min.	Max.	Unit	Condition
Module output SCL and SDA	V _{OL}	0	0.4	V	
Module Input SCL and SDA	V _{IL}	-0.3	V _{CC} *0.3	V	
	V _{IH}	V _{CC} *0.7	V _{CC} +0.5	V	
InitMode, ResetL and ModSelL	V _{IL}	-0.3	0.8	V	
	V _{IH}	2	V _{CC} +0.3	V	
IntL	V _{OL}	0	0.4	V	
	V _{OH}	V _{CC} -0.5	V _{CC} +0.3	V	

PIN ASSIGNMENT



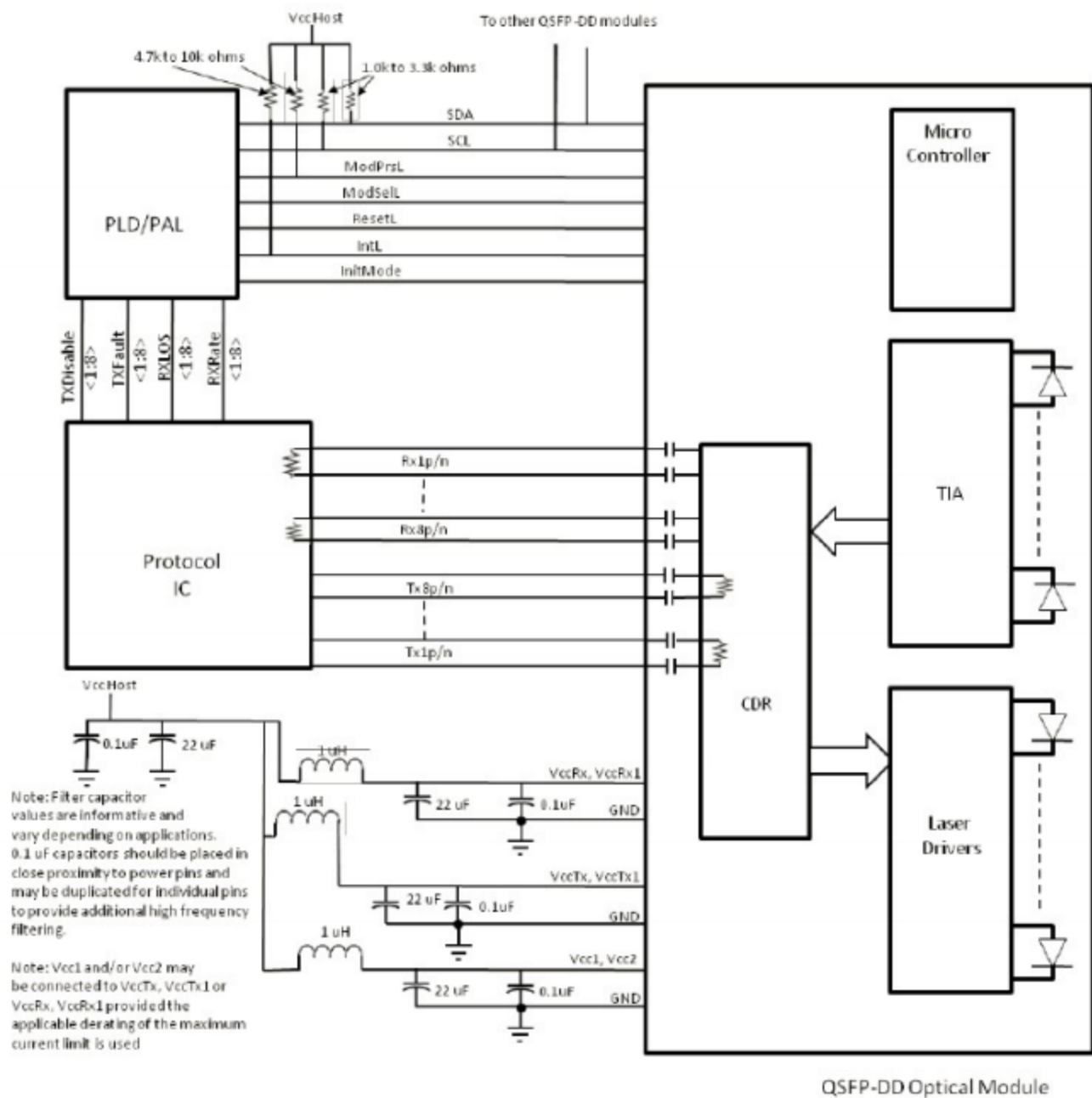
Pin definitions of the module high speed inputs/outputs



Active fibre ports in MPO-12 connector on module side

Pin	Logic	Symbol	Definition	Pin	Logic	Symbol	Definition
1		GND	Ground	39		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	42		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	45		GND	Ground
8	LVTTL-I	ModSelL	Module Select	46		Reserved	
9	LVTTL-I	ResetL	Module Reset	47		VS1	Module Vendor Specific 1
10		VccRx	+3.3V Power Supply Receiver	48		VccRx1	3.3V Power Supply
11	LVC MOS -I/O	SCL	2-wire serial interface clock	49		VS2	Module Vendor Specific 2
12	LVC MOS -I/O	SDA	2-wire serial interface data	50		VS3	Module Vendor Specific 3
13		GND	Ground	51		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	57		GND	Ground
20		GND	Ground	58		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	59	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	60	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	61		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output	62	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	63	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	64		GND	Ground
27	LVTTL-O	ModPrsL	Module Present	65		NC	Not connected
28	LVTTL-O	IntL	Interrupt	66		Reserved	
29		VccTx	+3.3V Power Supply Transmitter	67		VccTx1	3.3V Power Supply
30		Vcc1	+3.3V Power Supply	68		Vcc2	3.3V Power Supply
31	LVTTL-I	InitMode	Initialization mode	69		Reserved	
32		GND	Ground	70		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	71	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	72	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	73		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	74	CML-I	Tx5p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input	75	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	76		GND	Ground

RECOMMENDED HOST BOARD



Recommended QSFP-DD Host Board Schematic

TIMING FOR SOFT CONTROL & STATUS FUNCTIONS

Parameter	Symbol	Min.	Max.	Unit
MgmtInit Duration		-	2000	ms
ResetL Assert Time	t_reset_init	10	-	µs
IntL Assert Time	ton_IntL	-	200	ms
IntL Deassert Time	toff_IntL	-	500	µs
Rx LOS Assert Time (optional fast mode)	ton_losf	-	1	ms
Tx Fault Assert Time	ton_Txfault	-	200	ms
Flag Assert Time	ton_flag	-	200	ms
Mask Assert Time	ton_mask	-	100	ms
Mask Deassert Time	toff_mask	-	100	ms

I/O TIMING FOR SQUELCH & DISABLE

Parameter	Symbol	Min.	Max.	Unit	Notes
Rx Squelch Assert Time	ton_Rxsq	-	150	ms	
Tx Squelch Assert Time	ton_Txsq	-	400	ms	
Tx Squelch Deassert Time	toff_Txsq	-	1.5	s	
Tx Disable Assert Time (optional fast mode)	ton_Txdisf	-	3	ms	
Tx Disable Deassert Time (optional fast mode)	toff_Txdisf	-	10	ms	
Rx Output Disable Assert Time	ton_Rxdis	-	100	ms	
Rx Output Disable Deassert Time	toff_Rxdis	-	100	ms	
Squelch Disable Assert Time	ton_sqdis	-	N/A		Not support
Squelch Disable Deassert Time	toff_sqdis	-	N/A		Not support

DIGITAL DIAGNOSTICS

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	°C	Internal
Voltage	0 to V _{CC}	3%	V	Internal
Tx Bias Current (Each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (Each Lane)	-1.9 to +4.8	±3	dB	Internal
Rx Receive Power (Each Lane)	-8.2 to +4.8	±3	dB	Internal

OPERATION MODE SWITCHOVER

The module can work at 4x100G or 1x400G operation modes. It works at 4x100G as the default mode after power-up. See below for how to switch operation mode:

To switch to 1x400G:

Step 1. Write A0 page 10h 80h to 0xFF

Step 2. Write A0 page 10h B2h to 0xFF

Step 3. Write A0 page 10h 80h to 0x00

To switch to 4x100G:

Step 1. Write A0 page 10h 80h to 0xFF

Step 2. Write A0 page 10h 8Fh to 0xFF

Step 3. Write A0 page 10h 80h to 0x00

MECHANICAL SPECIFICATIONS (UNIT: mm)

