



Statement of Volatility – Dell PowerEdge R470

Revision change list:

Revision	Change items	Notes
1.0	Releaser for RTS1.2 (June FY26)	

Dell PowerEdge R470 contains both volatile and non-volatile (NV) components. Volatile components lose their data immediately upon removal of power from the component. Non-volatile components continue to retain their data even after the power has been removed from the component. Components chosen as user-definable configuration options (those not soldered to the motherboard) are not included in the Statement of Volatility. Configuration option information (pertinent to options such as microprocessors, remote access controllers, and storage controllers) is available by component separately. The following NV components are present in the PowerEdge R470 server.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
HPM										
CPU Internal CMOS RAM	Volatile	1	U_CPU0	128 byte	PIROM	No	Real-time clock and BIOS configuration settings	BIOS	N/A – BIOS only control	1) Set NVRAM_CLR jumper to clear BIOS configuration settings at boot and reboot system. 2) Power off the system, remove coin cell battery for 30 seconds, replace battery and then power back on. 3) Restore default configuration in F2 system setup menu.
FRU EEPROM	Non-Volatile	1	U8	32 KB	EEPROM	YES	Boot code, system configuration information	I2C	Software writes protected	Not possible with any utilities or applications and system is not functional if corrupted or removed.
RTC IC	Non-Volatile	1	U7	128 Bytes RAM for host CPU and BMC. 16 Bytes	Battery Backup SRAM	No	Remember real-time clock, calendar	Not utilized	Not accessible	RTC_CLR# active Low Input to clear backed RAM.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
				RAM for BMC only.						
System CPLD RAM	Volatile	1	U11	512 KB	RAM	Yes	Not utilized	Not utilized	Not accessible	Not accessible
System Memory: RDIMM	Volatile	16	CPU0: A1 ~ A16	Up to 256GB per DIMM	RAM	Yes	System OS RAM	System OS	OS Control	Reboot or power down system
CPU_VR	Non-Volatile	3	PU1,PU10,PU13		NVM	Yes	Boot code, system configuration information	I2C	Software writes protected	Not possible with any utilities or applications and system is not functional if corrupted or removed.
CPU_VCCF A	Non-Volatile	1	PU16		NVM	Yes	Boot code, system configuration information	I2C	Software writes protected	Not possible with any utilities or applications and system is not functional if corrupted or removed.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
DC-SCM										
BIOS SPI Flash	Non-Volatile	1	U11	64 MB	SPI Flash	No	Boot code, system configuration information, UEFI environment	SPI interface via CPU	Software writes protected	Not possible with any utilities or applications and system is not functional if corrupted or removed.
BIOS Data SPI Flash	Non-Volatile	1	U14	32 MB	SPI Flash	No	32MB Data SPI ROM storage BIOS setting.	SPI interface via CPU	Software writes protected	Not possible with any utilities or applications and the system is not functional if BIOS SPI is corrupted or removed.
iDRAC SPI Flash	Non-Volatile	1	U57	8 MB	SPI Flash	No	iDRAC/OSM Uboot (boot loader), server management persistent store (i.e. iDRAC/OSM boot variables), and virtual planar FRU	SPI interface via iDRAC/OSM	Embedded iDRAC/OSM subsystem firmware actively controls sub area based write protection as needed.	The user cannot clear memory completely. However, user data, lifecycle log and archive, SEL, and firmware image repository can be cleared using Delete Configuration and Retire System, which can be accessed through the

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
										Lifecycle Controller interface.
BMC EMMC	Non-Volatile	1	U3	16 GB	eMMC NAND Flash	No	Operational iDRAC/OSM FW, Lifecycle Controller (LC) USC partition, LC service diags, LC OS drivers, USC firmware, iDRAC/OSM MAC Address, and EPPID, rac log, System Event Log, lifecycle log cache	NAND Flash interface via iDRAC/OSM	Embedded FW write protected	The user cannot clear memory completely. However, user data, lifecycle log and archive, SEL, and firmware image repository can be cleared using Delete Configuration and Retire System, which can be accessed through the Lifecycle Controller interface.
iDRAC/OS M DDR4	Volatile	1	U2	16Gb	RAM	Yes	iDRAC/OSM RAM	iDRAC/OSM firmware	Not write-protected	Remove AC

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
1U RCP										
MCU	Non-Volatile	1	U8 (Renesas) U9 (Cypress)	32KB	FLASH	No	Feature Control Firmware	I2C Interface via iDRAC/OSM	HW write protection for boot. No HW WP for APP FW	Not user clearable
EEPROM	Non-Volatile	1	U3	32Mb	SPI Flash	No	SPI flash device to store information about the system Service Tag, system configuration, or iDRAC license	SPI interface via iDRAC/OSM	No, HW disable WP	SPI interface via iDRAC/OSM
LCP KVM										
MCU	Non-Volatile	1	U10	32KB	FLASH	No	Feature Control Firmware	I2C Interface via iDRAC/OSM	HW write protection for boot. No HW WP for APP FW	Not user clearable
LCP Quick Sync Board										

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
MCU	Non-Volatile	1	U1	2048KB	FLASH	No	Feature Control Firmware	I2C Interface via iDRAC/OSM	HW write protection for boot. No HW WP for APP FW	Not user clearable

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
1U/ 2U Rigid Riser Gen5										
EEPROM	Non-Volatile	1	U13	1kb/2kb	I2C Flash	No	FRU ROM	Program via I2C	Software writes protected	Not user clearable
Cable Riser										
EEPROM	Non-Volatile	1	U13	1kb/2kb	I2C Flash	No	FRU ROM	Program via I2C	Software writes protected	Not user clearable

Hybrid Riser										
EEPROM	Non-Volatile	1	U13	1kb/2kb	I2C Flash	No	FRU ROM	Program via I2C	Software writes protected	Not user clearable

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
1U Fan										
MCU	Non-Volatile	1	U1	64KB	FLASH	No	Feature Control Firmware	I2C Interface via iDRAC/OSM	HW write protection for boot. No HW WP for APP FW	Not user clearable

[illegible]

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
1U 8x E3 G5x4 BP										
SEP internal flash	Non-Volatile	1	U_SEP	Flash: 512KB Code/data SRAM:416KB (352KB for code; 64KB for data) Battery Powered Storage SRAM:128B	Integrated Flash +Data SRAM + Battery Powered Storage SRAM	No	Firmware + FRU	I2C interface via OSM	Program write protect bit	The user cannot clear memory.
MCU	Non-volatile	2	U_MCU1, U_MCU2	Flash: 64KB Data SRAM :4096bytes	Integrated Flash + Data SRAM	No	Firmware	I2C interface via ESEP	Program write protect bit	User cannot clear the memory.
Backplane Internal FRU	Non-Volatile	1	U_SEP	512 Bytes	Integrated Flash +Data SRAM +Battery Powered	No	FRU	Programmed at ICT during production.	No write protected	The user cannot clear memory.

					Storage SRAM					
1U 8x Uni BP										
SEP internal flash	Non- Volatile	1	U_SEP	Flash: 512KB Code/data SRAM:416KB (352KB for code; 64KB for data) Battery Powered Storage SRAM:128B	Integrated Flash +Data SRAM + Battery Powered Storage SRAM	No	Firmware + FRU	I2C interface via OSM	Program write protect bit	The user cannot clear memory.
MCU	Non- volatile	2	U_MCU1, U_MCU2	Flash: 64KB Data SRAM :4096bytes	Integrated Flash + Data SRAM	No	Firmware	I2C interface via ESEP	Program write protect bit	User cannot clear the memory.
Backplane Internal FRU	Non- Volatile	1	U_SEP	512 Bytes	Integrated Flash +Data SRAM +Battery Powered Storage SRAM	No	FRU	Programmed at ICT during production.	No write protected	The user cannot clear memory.
1U 10x Uni BP										

SEP internal flash	Non-Volatile	1	U_SEP	Flash: 512KB Code/data SRAM:416KB (352KB for code; 64KB for data) Battery Powered Storage SRAM:128B	Integrated Flash +Data SRAM + Battery Powered Storage SRAM	No	Firmware + FRU	I2C interface via iDRAC	Program write protect bit	The user cannot clear memory.
MCU	Non-volatile	3	U_MCU1, U_MCU2, U_MCU3	Flash: 64KB Data SRAM :4096bytes	Integrated Flash + Data SRAM	No	Firmware	I2C interface via ESEP	Program write protect bit	User cannot clear the memory.
Backplane Internal FRU	Non-Volatile	1	U_SEP	512 Bytes	Integrated Flash +Data SRAM +Battery Powered Storage SRAM	No	FRU	Programmed at ICT during production.	No write protected	The user cannot clear memory.
1U 4x3.5 SASBP										
SEP internal flash	Non-Volatile	1	U_SEP	Flash: 512KB Code/data SRAM:416KB (352KB for code; 64KB for data) Battery Powered	Integrated Flash +Data SRAM + Battery Powered	No	Firmware + FRU	I2C interface via iDRAC	Program write protect bit	The user cannot clear memory.

				Storage SRAM:128B	Storage SRAM					
MCU	Non- volatile	1	U_MCU1,	Flash: 64KB Data SRAM :4096bytes	Integrated Flash + Data SRAM	No	Firmware	I2C interface via ESEP	Program write protect bit	User cannot clear the memory.
Backplane Internal FRU	Non- Volatile	1	U_SEP	512 Bytes	Integrated Flash +Data SRAM +Battery Powered Storage SRAM	No	FRU	Programmed at ICT during production.	No write protected	The user cannot clear memory.
1U 2xE3 Rear BP										
SEP internal flash	Non- Volatile	1	U_SEP	Flash: 512KB Code/data SRAM:416KB (352KB for code; 64KB for data) Battery Powered Storage SRAM:128B	Integrated Flash +Data SRAM + Battery Powered Storage SRAM	No	Firmware + FRU	I2C interface via iDRAC	Program write protect bit	The user cannot clear memory.
MCU	Non- volatile	1	U_MCU1,	Flash: 64KB Data SRAM :4096bytes	Integrated Flash + Data SRAM	No	Firmware	I2C interface via ESEP	Program write protect bit	User cannot

										clear the memory.
Backplane Internal FRU	Non-Volatile	1	U_SEP	512 Bytes	Integrated Flash +Data SRAM +Battery Powered Storage SRAM	No	FRU	Programmed at ICT during production.	No write protected	The user cannot clear memory.
Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
H965i Front DC-MHS PERC (Internal Controller)										
SPI Flash	Non-Volatile	1	U2	256Mb	SPI Flash	No	Card firmware	Pre-programmed before assembly. Can be updated using Dell/Broadcom tools	Not write protected. Not visible to Host Processor	User cannot clear the memory.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
FRU	Non-volatile	1	U1020	2Kb	EEPROM	No	Card manufacturing information	Programmed at ICT during production.	Not write protected	User cannot clear the memory.
CPLD	Non-volatile	1	U1088	64kb	Flash	No	Power sequencing and Cache Offload	Controller may program data during FW update	Not write protected Not visible to host CPU	User cannot clear this memory
NVSRAM	Non-volatile	1	U1087	1Mb	NVSRAM	No	Configuration data	ROC writes configuration data to NVSRAM	Not write protected Not visible to host CPU	User cannot clear this memory
BMU	Non-Volatile	1	U1126	180KB	Integrated Flash	No	Battery Management control	ROC may program data during FW and during boot	Not write protected	User cannot clear this memory
Battery FRU	Non-Volatile	1	U2	256byte	EEPROM	No	Battery FRU	Battery vendor program MFG data before ship out to ODM.	Not write protected	User cannot clear this memory
SPD	Non-volatile	1	U22	2Kb	temp sensor with integrated	No	Memory configuration data	Pre-programmed	No write protected. Not	User cannot clear the memory.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
					SPD EEPROM			before assembly	visible to Host Processor	
NAND Flash	Non-volatile	1	U1100	512Gb	NAND Flash	No	Cache offload during unexpected power loss	Programmed by ROC during cache offload	No write protected. Not visible to Host Processor	User cannot clear the memory.
SDRAM	Volatile	10	U1077 U1078 U1079 U1080 U1081 U1082 U1083 U1084 U1085 U1086	512Mb x16	SDRAM	No	Cache for HDD I/O	ROC writes to this memory - using it as cache for data IO to HDDs	No write protected. Not visible to Host Processor	Cache can be cleared by powering off the card
H965i PERC Adapter										
SPI Flash	Non-Volatile	1	U2	256Mb	SPI Flash	No	Card firmware	Pre-programmed before assembly. Can be updated	Not write protected. Not visible to Host Processor	User cannot clear the memory.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
								using Dell/LSI tools		
FRU	Non-volatile	1	U1019	2Kb	EEPROM	No	Card manufacturing information	Programmed at ICT during production.	Not write protected	User cannot clear the memory.
CPLD	Non-volatile	1	U1088	64kb	Flash	No	Power sequencing and Cache Offload	Controller may program data during FW update	Not write protected Not visible to host CPU	User cannot clear this memory
BMU	Non-Volatile	1	U1126	180KB	Integrated Flash	No	Battery Management control	ROC may program data during FW and during boot	Not write protected	User cannot clear this memory
Battery FRU	Non-Volatile	1	U2	256byte	EEPROM	No	Battery FRU	Battery vendor program MFG data before ship out to ODM.	Not write protected	User cannot clear this memory
NVSRAM	Non-volatile	1	U1087	1Mb	NVSRAM	No	Configuration data	ROC writes configuration data to NVSRAM	Not write protected Not visible to host CPU	User cannot clear this memory

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
SPD	Non-volatile	1	U22	2Kb	EEPROM	No	Memory configuration data	Pre-programmed before assembly	No write protected. Not visible to Host Processor	User cannot clear the memory.
NAND Flash	Non-volatile	1	U1100	512Gb	NAND Flash	No	Cache offload during unexpected power loss	Programmed by ROC during cache offload	No write protected. Not visible to Host Processor	User cannot clear the memory.
SDRAM	Volatile	10	U1077 U1078 U1079 U1080 U1081 U1082 U1083 U1084 U1085 U1086	512Mb x16	SDRAM	No	Cache for HDD I/O	ROC writes to this memory - using it as cache for data IO to HDDs	No write protected. Not visible to Host Processor	Cache can be cleared by powering off the card
H365i PERC Front DC-MHS (Internal Controller)										
SPI Flash	Non-Volatile	1	U2	256Mb	SPI Flash	No	Card firmware	Pre-programmed before	Not write protected. Not	User cannot clear the memory.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
								assembly. Can be updated using Dell/Broadcom tools	visible to Host Processor	
FRU	Non-volatile	1	U1020	2Kb	EEPROM	No	Card manufacturing information	Programmed at ICT during production.	Not write protected	User cannot clear the memory.
CPLD	Non-volatile	1	U1088	64kb	Flash	No	Power sequencing	Controller may program data during FW update	Not write protected Not visible to host CPU	User cannot clear this memory
NVSRAM	Non-volatile	1	U1087	1Mb	NVSRAM	No	Configuration data	ROC writes configuration data to NVSRAM	Not write protected Not visible to host CPU	User cannot clear this memory
H365i PERC Adapter										
SPI Flash	Non-Volatile	1	U2	256Mb	SPI Flash	No	Card firmware	Pre-programmed before assembly. Can be updated	Not write protected. Not visible to Host Processor	User cannot clear the memory.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
								using Dell/Broadcom tools		
FRU	Non-volatile	1	U1019	2Kb	EEPROM	No	Card manufacturing information	Programmed at ICT during production.	Not write protected	User cannot clear the memory.
CPLD	Non-volatile	1	U1088	64kb	Flash	No	Power sequencing	Controller may program data during FW update	Not write protected Not visible to host CPU	User cannot clear this memory
NVSRAM	Non-volatile	1	U1087	1Mb	NVSRAM	No	Configuration data	ROC writes configuration data to NVSRAM	Not write protected Not visible to host CPU	User cannot clear this memory

BOSS-N1 DC-MHS (Internal Controller)										
SPI Flash	Non-Volatile	1	U7	16MB	SPI Flash	No	BOSS controller (Nevox) FW	Offline programmed by copy machine.	NA	User cannot clear the memory.

FRU	Non-volatile	1	U13	2Kbit	EEPROM	No	BOSS Card information including Power/Thermal/manufacturing information	Static: offline programmed by copy machine Dynamic: online programmed by ICT	NA	User cannot clear the memory.
S-MCU	Non-volatile	1	U15	32KB	EEPROM	No	FW Security purpose	Offline programmed by copy machine.	NA	User cannot clear the memory.



NOTE: For any information that you may need, direct your questions to your Dell Marketing contact.

06 - 2025

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