



**GR 667 D2 64 L5 4G**

GOODRAM  
SPEED/DATATRANSFER 667MHz/PC2-5300  
MODULE TYPE DDR2 SDRAM DIMM  
MODULE DATA WIDTH 64  
CAS LATENCY 5  
MODULE DENSITY 4GB

**DDR II MODULE  
PART NUMBERING  
SYSTEM**

## FEATURES

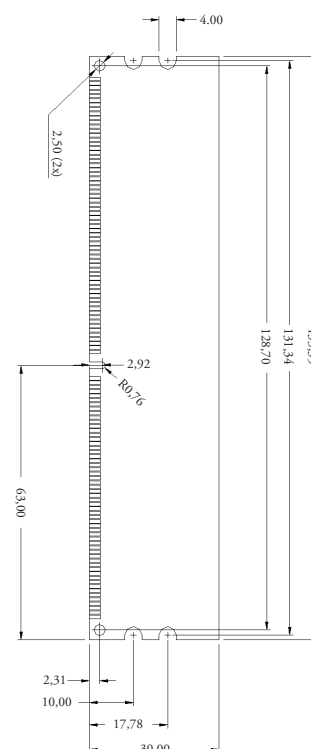
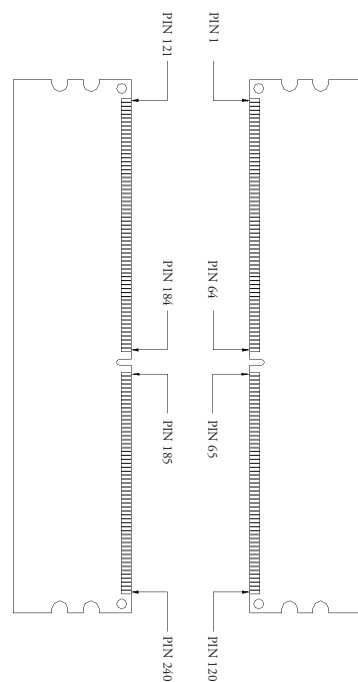
|                        |                 |
|------------------------|-----------------|
| PART NUMBER            | GR667D264L5/4G  |
| MODULE TYPE            | DDR2 SDRAM DIMM |
| MODULE DENSITY         | 4GB             |
| MODULE DATA WIDTH      | 64              |
| DRAM CHIP ORAGNIZATION | 256Mx8          |
| NUMBER OF DRAM CHIPS   | 16              |
| NUMBER OF MODULE RANKS | 2               |
| NUMBER OF MODULE SIDES | 2               |
| REGISTERED             | NO              |
| ECC SUPPORT            | NO              |
| PIN COUNT              | 240 PIN         |
| SUPPLY VOLTAGE         | 1,8V            |
| SSTL_18 COMPATIBLE     | YES             |

## DYNAMIC PARAMETERS FOR 667MHz

|                                             |    |
|---------------------------------------------|----|
| CAS LATENCY                                 | 5  |
| RAS# TO CAS# DELAY, t <sub>RC</sub> D       | 5  |
| ROW PRECHARGE TIME, t <sub>RP</sub>         | 5  |
| ACTIVE TO PRECHARGE TIME, t <sub>TRAS</sub> | 15 |

## PCB DETAILS

|                          |                       |
|--------------------------|-----------------------|
| PCB TYPE                 | DDR2 SDRAM DIMM       |
| BOARD DIMENSIONS         | 133,35 x 30mm ± 0,1mm |
| BOARD THICKNESS          | 1,27mm ± 0,13mm       |
| DRAM PACKAGE INFORMATION | FBGA, x8bit           |
| CONTACT PADS (PIN)       | GOLD PLATED           |





| SPD CONFIGURATION |                                                                 |      |     |
|-------------------|-----------------------------------------------------------------|------|-----|
| BYTE              | DESCRIPTION                                                     | HEX  | DEC |
| 0                 | Number of Serial PD Bytes written during module production      | 0x80 | 128 |
| 1                 | Total number of Bytes in Serial PD device                       | 0x08 | 8   |
| 2                 | Fundamental Memory Type (FPM, EDO, SDRAM ...)                   | 0x08 | 8   |
| 3                 | Number of Row Addresses on this assembly                        | 0x0F | 15  |
| 4                 | Number of Column Addresses on this assembly                     | 0x0A | 10  |
| 5                 | Number of DIMM Banks                                            | 0x61 | 97  |
| 6                 | Data Width of this assembly                                     | 0x40 | 64  |
| 7                 | Data Width of this assembly                                     | 0x00 | 0   |
| 8                 | Voltage Interface Level of this assembly                        | 0x05 | 5   |
| 9                 | SDRAM Cycle time at Maximum Supported CAS Latency (CL), CL=X    | 0x30 | 48  |
| 10                | SDRAM Access from Clock                                         | 0x45 | 69  |
| 11                | DIMM configuration type (Non-parity, Parity or ECC)             | 0x00 | 0   |
| 12                | Refresh Rate/Type                                               | 0x82 | 130 |
| 13                | Primary SDRAM Width                                             | 0x08 | 8   |
| 14                | Error Checking SDRAM Width                                      | 0x00 | 0   |
| 15                | SDRAM Device Attributes: Minimum Clock Delay, Back-to-Back RCA  | 0x00 | 0   |
| 16                | SDRAM Device Attributes: Burst Lengths Supported                | 0x0C | 12  |
| 17                | SDRAM Device Attributes: Number of Banks on SDRAM Device        | 0x08 | 8   |
| 18                | SDRAM Device Attributes: CAS Latency                            | 0x38 | 56  |
| 19                | SDRAM Device Attributes: CS Latency                             | 0x01 | 1   |
| 20                | SDRAM Device Attributes: Write Latency/DIMM Type Information    | 0x02 | 2   |
| 21                | SDRAM Module Attributes                                         | 0x00 | 0   |
| 22                | SDRAM Device Attributes: General                                | 0x03 | 3   |
| 23                | Minimum Clock Cycle at CL = X - 0.5                             | 0x3D | 61  |
| 24                | Maximum Data Access Time (tAC) from Clock at CL = X - 0.5       | 0x50 | 80  |
| 25                | Minimum Clock Cycle at CL = X - 1                               | 0x50 | 80  |
| 26                | Maximum Data Access Time (tAC) from Clock at CL = X - 1         | 0x60 | 96  |
| 27                | Minimum Row Precharge Time (tRP)                                | 0x3C | 60  |
| 28                | Minimum Row Active to Row Active delay (tRRD)                   | 0x1E | 30  |
| 29                | Minimum RAS to CAS delay (tRCD)                                 | 0x3C | 60  |
| 30                | Minimum Active to Precharge Time (tRAS)                         | 0x2D | 45  |
| 31                | Module Bank Density                                             | 0x02 | 2   |
| 32                | Address and Command Input Setup Time Before Clock               | 0x20 | 32  |
| 33                | Address and Command Input Hold Time After Clock                 | 0x27 | 39  |
| 34                | Data Input Setup Time Before Clock                              | 0x10 | 16  |
| 35                | Data Input Hold Time After Clock                                | 0x17 | 23  |
| 36                | Write recovery time (tWR)                                       | 0x3C | 60  |
| 37                | Internal write to read command delay (tWTR)                     | 0x1E | 30  |
| 38                | Internal read to precharge command delay (tRTP)                 | 0x1E | 30  |
| 39                | Memory Analysis Probe Characteristics                           | 0x00 | 0   |
| 40                | Extension of Byte 41 tRC and Byte 42 tRFC                       | 0x00 | 0   |
| 41                | SDRAM Device Minimum Active to Active/Auto Refresh Time (tRC)   | 0x3C | 60  |
| 42                | SDRAM Device Minimum Auto Refresh to Active/Auto Refresh (tRFC) | 0xC5 | 197 |
| 43                | SDRAM Device Maximum device cycle time (tCKmax)                 | 0x80 | 128 |
| 44                | SDRAM Device Maximum skew between DQS and DQ signals (tDQSQ)    | 0x18 | 24  |
| 45                | DDR SDRAM Device Maximum Read Data Hold Skew Factor (tQHS)      | 0x22 | 34  |
| 46                | Reserved for future use                                         | 0x0F | 15  |
| 47                | SDRAM Device Attributes - DDR SDRAM DIMM Height                 | 0x50 | 80  |
| 48                | Reserved for future use                                         | 0x60 | 96  |
| 49                | Reserved for future use                                         | 0x5F | 95  |
| 50                | Reserved for future use                                         | 0x44 | 68  |
| 51                | Reserved for future use                                         | 0x43 | 67  |
| 52                | Reserved for future use                                         | 0x31 | 49  |
| 53                | Reserved for future use                                         | 0x49 | 73  |
| 54                | Reserved for future use                                         | 0x2F | 47  |
| 55                | Reserved for future use                                         | 0x72 | 114 |
| 56                | Reserved for future use                                         | 0x3A | 58  |
| 57                | Reserved for future use                                         | 0x43 | 67  |
| 58                | Reserved for future use                                         | 0x00 | 0   |
| 59                | Reserved for future use                                         | 0x00 | 0   |
| 60                | Reserved for future use                                         | 0x00 | 0   |
| 61                | Reserved for future use                                         | 0x00 | 0   |
| 62                | SPD Revision                                                    | 0x12 | 18  |
| 63                | Checksum for Bytes 0-62                                         | 0x92 | 146 |
| 64-255            | Manufacturer's specific data                                    |      |     |

