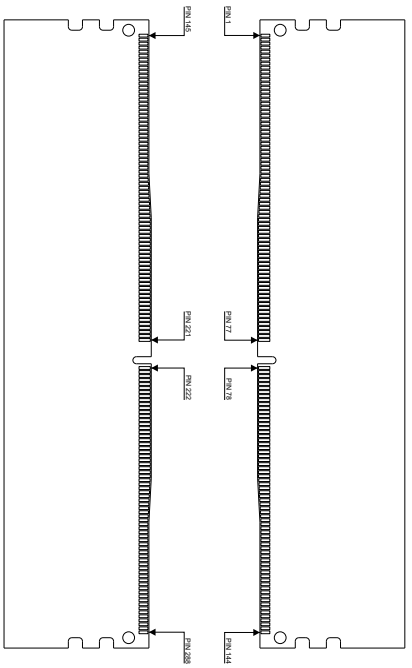
GYR 2400 D4 64 L15 S 4G

- GYR — GOODRAM PLAY RED
- 2400 — SPEED / DATA TRANSFER 2400MHz / PC4-19200
- D4 — MODULE TYPE DDR4 SDRAM DIMM
- 64 — MODULE DATA WIDTH 64
- L15 — CAS LATENCY 15
- S — SINGLE RANK
- 4G — MODULE DENSITY 4GB

DDR IV MODULE PART NUMBERING SYSTEM



FEATURES

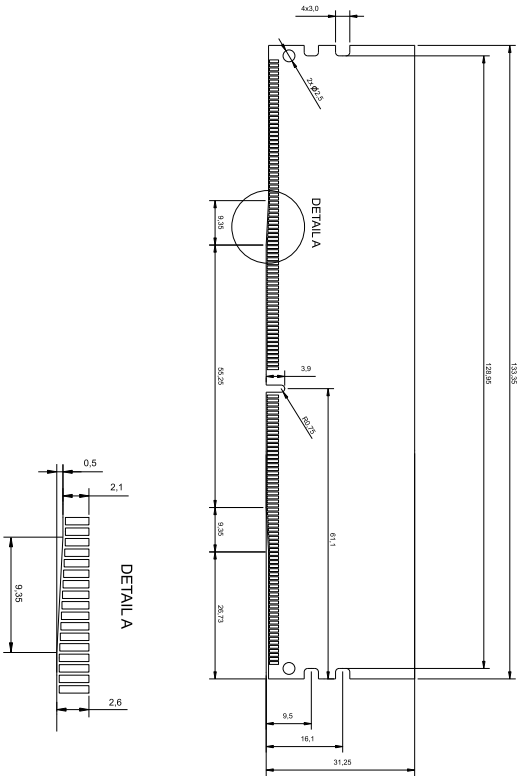
PART NUMBER	GYR2400D464L15S/4G
MODULE TYPE	DDR4 SDRAM DIMM
MODULE DENSITY	4GB
MODULE DATA WIDTH	64
DRAM COMPONENT ORAGNIZATION	512Mx8
NUMBER OF DRAM COMPONENTS	8
NUMBER OF MODULE RANKS	1
NUMBER OF MODULE SIDES	1
REGISTERED	NO
ECC SUPPORT	NO
PIN COUNT	288 PIN
SUPPLY VOLTAGE	1,2V
INTERFACE	PSEUDO OPEN DRAIN 1.2V (POD12)

DYNAMIC PARAMETERS FOR 2400MHz

CAS LATENCY	15
RAS# TO CAS# DELAY, tRCD	15
ROW PRECHARGE TIME, tRP	15
ACTIVE TO PRECHARGE TIME, tRAS	35

PCB DETAILS

PCB TYPE	DDR4 SDRAM DIMM
BOARD DIMENSIONS	133,35 x 31,25mm ± 0,1mm
BOARD THICKNESS	1,4mm ± 0,1mm
DRAM PACKAGE INFORMATION	FBGA, x8bit
CONTACT PADS (PIN)	GOLD PLATED



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SPD CONFIGURATION

BYTE	DESCRIPTION	HEX	DEC
0	Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage 1 2	0x23	35
1	SPD Revision	0x10	16
2	Key Byte / DRAM Device Type	0x0c	12
3	Key Byte / Module Type	0x02	2
4	SDRAM Density and Banks	0x84	132
5	SDRAM Addressing	0x19	25
6	SDRAM Package Type	0x00	0
7	SDRAM Optional Features	0x08	8
8	SDRAM Thermal and Refresh Options	0x00	0
9	Other SDRAM Optional Features	0x00	0
10	Reserved -- must be coded as 0x00	0x00	0
11	Module Nominal Voltage, VDD	0x03	3
12	Module Organization	0x01	1
13	Module Memory Bus Width	0x03	3
14	Module Thermal Sensor	0x00	0
15	Extended module type	0x00	0
16	Reserved -- must be coded as 0x00	0x00	0
17	Timebases	0x00	0
18	SDRAM Minimum Cycle Time (tCKAVGmin)	0x07	7
19	SDRAM Maximum Cycle Time (tCKAVGmax)	0x0c	12
20	CAS Latencies Supported, First Byte	0xfc	252
21	CAS Latencies Supported, Second Byte	0x03	3
22	CAS Latencies Supported, Third Byte	0x00	0
23	CAS Latencies Supported, Fourth Byte	0x00	0
24	Minimum CAS Latency Time (tAAmin)	0x64	100
25	Minimum RAS to CAS Delay Time (tRCDmin)	0x64	100
26	Minimum Row Precharge Delay Time (tRPmin)	0x64	100
27	Upper Nibbles for tRASmin and tRCmin	0x11	17
28	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	0x18	24
29	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	0x7c	124
30	Minimum Refresh Recovery Delay Time (tRFC1min), LSB	0x20	32
31	Minimum Refresh Recovery Delay Time (tRFC1min), MSB	0x08	8
32	Minimum Refresh Recovery Delay Time (tRFC2min), LSB	0x00	0
33	Minimum Refresh Recovery Delay Time (tRFC2min), MSB	0x05	5
34	Minimum Refresh Recovery Delay Time (tRFC4min), LSB	0x70	112
35	Minimum Refresh Recovery Delay Time (tRFC4min), MSB	0x03	3
36	Minimum Four Activate Window Time (tFAWmin), Most Significant Nibble	0x00	0
37	Minimum Four Activate Window Time (tFAWmin), Least Significant Byte	0xa8	168
38	Minimum Activate to Activate Delay Time (tRRD_Smin), different bank group	0x1b	27
39	Minimum Activate to Activate Delay Time (tRRD_Lmin), same bank group	0x28	40
40	Minimum CAS to CAS Delay Time (tCCD_Lmin), same bank group	0x28	40
41-59	Reserved -- must be coded as 0x00	0x00	0
60	Connector to SDRAM Bit Mapping	0x16	22
61	Connector to SDRAM Bit Mapping	0x36	54
62	Connector to SDRAM Bit Mapping	0x16	22
63	Connector to SDRAM Bit Mapping	0x36	54
64	Connector to SDRAM Bit Mapping	0x16	22
65	Connector to SDRAM Bit Mapping	0x36	54
66	Connector to SDRAM Bit Mapping	0x16	22
67	Connector to SDRAM Bit Mapping	0x36	54
68	Connector to SDRAM Bit Mapping	0x00	0
69	Connector to SDRAM Bit Mapping	0x00	0
70	Connector to SDRAM Bit Mapping	0x2b	43
71	Connector to SDRAM Bit Mapping	0x0c	12
72	Connector to SDRAM Bit Mapping	0x2b	43
73	Connector to SDRAM Bit Mapping	0x0c	12
74	Connector to SDRAM Bit Mapping	0x2b	43
75	Connector to SDRAM Bit Mapping	0x0c	12
76	Connector to SDRAM Bit Mapping	0x2b	43
77	Connector to SDRAM Bit Mapping	0x0c	12

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SPD CONFIGURATION

BYTE	DESCRIPTION	HEX	DEC
78-116	Reserved -- must be coded as 0x00	0x00	0
117	Fine Offset for Minimum CAS to CAS Delay Time (tCCD_Lmin), same bank group	0x00	0
118	Fine Offset for Minimum Activate to Activate Delay Time (tRRD_Lmin), same bank group	0x9c	156
119	Fine Offset for Minimum Activate to Activate Delay Time (tRRD_Smin), different bank group	0xb4	180
120	Fine Offset for Minimum Activate to Activate/Refresh Delay Time (tRCmin)	0x00	0
121	Fine Offset for Minimum Row Precharge Delay Time (tRPmin)	0x00	0
122	Fine Offset for Minimum RAS to CAS Delay Time (tRCDmin)	0x00	0
123	Fine Offset for Minimum CAS Latency Time (tAAmin)	0x00	0
124	Fine Offset for SDRAM Maximum Cycle Time (tCKAVGmax)	0x00	0
125	Fine Offset for SDRAM Minimum Cycle Time (tCKAVGmin)	0xd6	214
126	CRC for Base Configuration Section, Least Significant Byte	0xef	239
127	CRC for Base Configuration Section, Most Significant Byte	0x5d	93
128-511	Module Specific Data		

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