

DDR4 Memory Technology on HP Z Workstations



DDR4 is the latest memory technology available for main memory on mobile, desktops, workstations, and server computers. DDR stands for Double Data Rate, which transfers data on both the rising and falling edges of the clock signal. DDR4 supports higher speeds and bandwidths than its predecessor DDR3 and enables significant power savings. Also, with the introduction of three dimensional stacking, it can support higher density DIMMs. It is not forward or backward compatible with any other type of RAM. DDR4 is supported on the HP Z1 G3, HP Z240, HP Z440, HP Z640, and HP Z840 Workstations.

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DDR4 Interface

The DDR4 memory interface connects the Dual In-line Memory Module (DIMM) to the CPU and consists of address/command and data bus groups. The data bus group is comprised of 64 bits on non-ECC systems and 72 bits on processors and systems that support ECC memory.

Memory Module makeup

A DDR4 DIMM consists of a number of distinct parts or components such as: Printed Circuit Board (PCB), DRAM chips, buffer register in the case of RDIMMs and LR DIMMs, and various discrete components. The DRAM chips used define the principal characteristics of a DIMM.

DRAM characteristics

Dynamic Random Access Memory (DRAM) chips come in different capacities. Today, 4 Gigabit (Gb) DRAMs are the most common and considered to be the best value. 8 Gb DRAMs are available, but carry a price premium.

DRAM chips can support 4, 8, or 16 data bits of width per chip. The width of the DRAM is designated by x#. For example, a 4 bit width DRAM is x4. The size and the width of a DRAM provide flexibility in creating DIMMs of different organisations to create the optimal DIMM at each capacity for each type. Since some DRAMs are single, dual or quad dies, the number of chips on a DIMM is an unreliable way to guess the type of DRAM used.

Three dimensional stacking or 3DS, is a new IC packaging technology that uses die stacking technology. 3DS allows for stacking of multiple DRAMs to support larger capacities at a lower cost and better performance.

ECC protection

Error Correction Code (ECC) provides protection against some data bit corruption events, either in the DRAM chips on the DIMM, or on the memory bus and in the platform's memory controller. On ECC DIMMs, 8 additional data bits are implemented, giving a data bus width of 72 bits instead of 64 bits as on non-ECC DIMMs.

Additional DRAM chips provide the additional memory space needed for the ECC protection. For each data transfer to the DIMM during a write event, an ECC code is calculated by the memory controller and stored along with the data to be written. On subsequent reads, the memory controller checks the ECC code and can determine if single-bit or multiple-bit errors occurred. It will correct single-bit errors automatically, thereby avoiding propagation of corrupted data to the system. Multi-bit errors cannot be corrected on platforms with independent memory channels, as in the case on most current workstation systems. However, multi-bit errors can be detected and, on HP Workstations, will immediately trigger a Machine Check event which will halt the operating system, thus preventing the propagation of corrupted data.

Non-ECC DIMMs have no extra data bits and so do not provide this added protection against incorrect data bit values. Non-ECC memory does not detect or correct single-bit or multi-bit errors. This can lead to system crashes, or data corruption without alerting the user. Data corruption can take many forms, such as: applications processing incorrect data, delivering incorrect results, application crashes, or file corruption. File corruption can lead to an inability to reopen a file, or the need to reinstall either an application or the operating system. ECC improves protection against corruption of data in memory and should be used in mission-critical applications or high-reliability, 24x7x365 environments.

Ranks

A Rank is defined to be a group of DRAM chips with matching characteristics such that the sum of the DRAM widths is either 64 bits (non-ECC) or 72 bits (ECC). Two examples are:

- 1 Rank = 8 x [x8 DRAM] = 64 bits
- 1 Rank = 18 x [x4 DRAM] = 72 bits

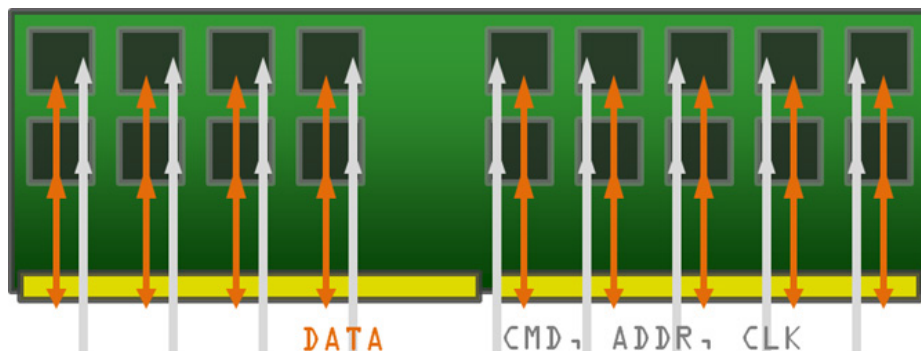
To increase capacity on a DIMM, additional ranks can be added. A memory rank is a set of DRAMs connected by a chip select line. This allows multiple DRAMs to be selected at the same time, so that each can provide their share (4, 8, or 16 data bits) of the 64 or 72 bit bus width.

DDR4 Memory Module types

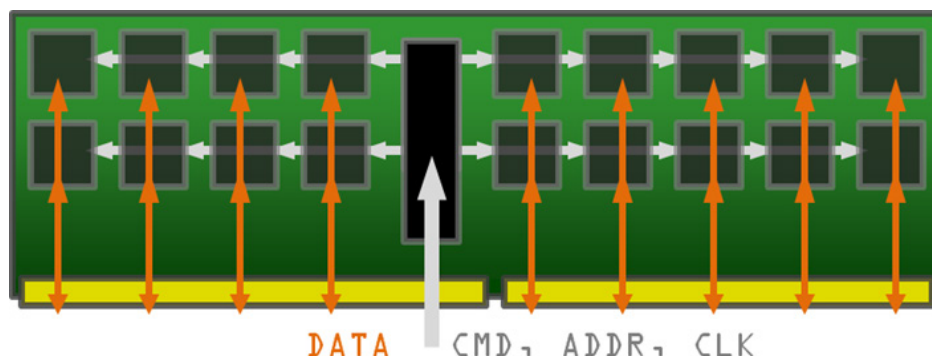
There are three types of DIMMs supported in HP Workstations, depending upon specific platform model support: unbuffered, registered, and load reduced. Note that these DIMM types cannot be intermixed in a system.

Unbuffered DIMMs (UDIMMs) are high volume DIMMs used in most consumer and entry enterprise applications. As the name implies, none of the signals are buffered. The data and command/address signals go directly into the DRAMs, as shown in the figure below. All UDIMMs support parity protection on the command and address signals. There are two types of UDIMMs: non-ECC and ECC. Non-ECC UDIMMs can support x8 and x16 DRAMs. ECC UDIMMs can only support x8 DRAMs.

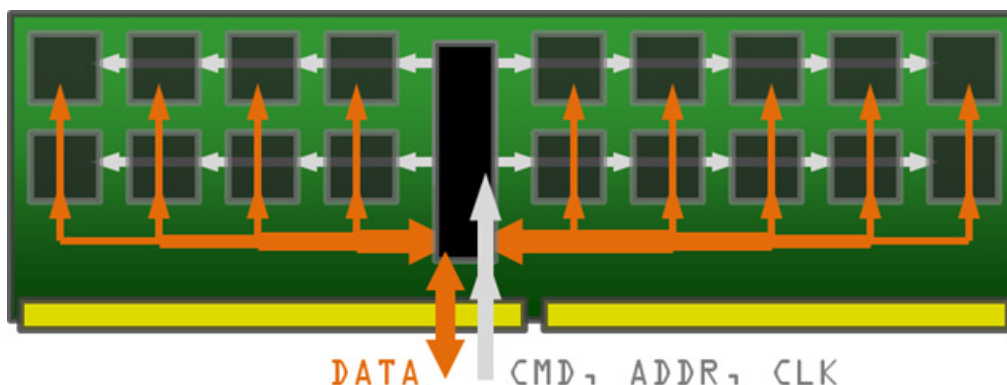
There are two different types of UDIMM form factors: Standard DIMMs and Small Outlined (SO) DIMMs. Standard DIMMs are found in most desktop workstations where space is not a concern. SO DIMMs are a smaller version of a DIMM. They are usually used in laptops and desktops workstations that are tight with space.



Registered DIMMs (RDIMMs) use registers to buffer the command and address signals, as shown in the figure below. The data bits are not buffered. All RDIMMs support ECC as well as parity protection on the command and address signals. RDIMMs should be used for higher reliability and for cost savings on higher capacities. Both x8 and x4 DRAMs can be supported, allowing larger memory capacities than UDIMMs by essentially doubling the number of DRAM chips which can be installed on a DIMM. RDIMMs can also present a large price advantage compared to large capacity UDIMMs as new DRAM chip density carries a price premium over the current high volume DRAM density.



Load Reducing DIMMs (LR DIMMs) are a newer technology that use registers to buffer command, address, and data signals, as shown in the figure below. ECC and parity are supported on LR DIMMs. LR DIMMs were created to reduce the electrical load on the system's memory data bus to a single load. This buffering architecture removes some of the speed and signal integrity limitations experienced with RDIMMs, and enables added capacity at increased speeds. The reduced load enables the use of quad and octal rank DIMM architecture. Octal rank DIMMs double the memory capacity over a quad rank RDIMM. There are also power savings per Gigabyte and added clock latency when compared to an RDIMM. Only x4 DRAMs are supported. LR DIMMs should be used if high capacity memory using today's technology is desired.



Current available DIMM type support table

	Unbuffered Non ECC	Unbuffered ECC	Registered	LR DIMM
Single rank	X	X	X	
Dual rank	X	X	X	X
Quad rank			X	X
Octal rank				X
16 bit width DRAMs (x16)	X			
8 bit width DRAMs (x8)	X	X	X	
4 bit width DRAMs (x4)			X	X
ECC data protection on data		X	X	X
Parity protection on Command/Address	X	X	X	X
Buffered Command/Address/Clk			X	X
Buffered data				X
3DS Technology				X

Memory Module capacity calculation

As mentioned previously, capacity is calculated using DRAM characteristics, specifically technology, width, and the total number of ranks. ECC must be considered in calculating the amount of DRAMs needed, but the ECC DRAM(s) are only used to hold the ECC values and should not be counted as part of the actual data payload which defines the DIMM capacity.

To calculate the capacity of a DIMM, the type of DRAMs used must be understood. The width of the DRAM should be used to find the number of DRAMs needed to make up the data bus. The capacity per rank can then be calculated by multiplying the number of DRAMs by the size of the DRAM, and further divided by 8 to convert bits into bytes. The total DIMM capacity is finally calculated by multiplying the rank capacity and the number of ranks on the DIMM. Below are two examples:

• 8 GB unbuffered, dual-rank, ECC DIMM

- Rank width = [9 DRAM] x [x8 width] = 72 bits
- Rank capacity = [8 payload DRAM] x [4 Gb technology] / [8 bits] = 4 GB
- DIMM capacity = [2 ranks] x [4 GB per rank] = 8 GB

• 64 GB registered, quad-rank, ECC DIMM

- Rank width = [18 DRAM] x [x4 width] = 72 bits
- Rank capacity = [16 payload DRAM] x [8 Gb technology] / 8 bits = 16 GB
- DIMM capacity = [4 ranks] x [16 GB per rank] = 64 GB

The max capacity available today, with 8 Gb based RDIMMs, is 64 Gigabyte (GB).

Label decoder

The following should be used to understand key attributes about the type of memory that is loaded in a system. When looking at the DIMM label, you should see the following format:

gggGB pheRxff PC4v-wwwwaa-mccdt-bb

- ggg = Module total capacity, in gigabytes
- phe = Number of package ranks of memory installed and number of logical ranks per package rank.
 - p = # of package ranks installed
 - h = DRAM package type
 - e = Logical ranks per package rank

- ff = Device organisation (data bid width, e.g. x4, x8, x16)
- PC4v = Indicates that this is a DDR4 module and the supported component supply voltage
 - PC4 = operates at 1.2V
 - PC4L = operates at a lower voltage TBD
- www = Module Speed in MHz pin
- aa = SDRAM speed grade
- m = module type
 - U = Unbuffered
 - E = ECC unbuffered
 - R = Registered
 - L = LR DIMM
- cc = Reference design file used in this design
- d = Revision number of the reference design used
- bb = JEDEC SPD Revision Encoding and additions level used on this DIMM

Learn more at

Tezzaron Semiconductor: Soft Errors in Electronic Memory: White Paper 2004
http://www.tezzaron.com/about/papers/soft_errors_1_1_secure.pdf

University of Toronto Study: DRAM Errors in the Wild:
A large-Scale Field Study; A cooperative study with Google of DRAM failures in actual use.
<http://www.cs.utoronto.ca/~bianca/papers/sigmetrics09.pdf>

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